ECMA-40, 2nd edition, High-Level Data Link Control Procedures (HDLC)-Frame Structure

SCOPE

This Standard defines in detail the frame structure for bit oriented High-Level Data Link Control (HDLC). It defines the relative positions of the various components of the basic frame and the bit combination for the frame delimiting sequence (Flag).

The bit insertion/deletion mechanism which is used to achieve total transparency within the frame is defined as well as the abort sequence and data channel states. The document also specifies the Frame Checking Sequence (FCS). No details of the encoding of the address and control field are included in this specification. These will be the subject of separate standards.