ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-103

PHYSICAL LAYER AT THE BASIC ACCESS INTERFACE BETWEEN DATA PROCESSING EQUIPMENT AND PRIVATE CIRCUIT SWITCHING NETWORKS

September 1985

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BRIEF HISTORY

This Standard ECMA-103 is one of a series of standards for the connection of data processing equipment to private circuit switching networks.

It uses the ISDN concepts as developed by CCITT and it is also within the framework of standards for open systems interconnection as defined by ISO 7498 and within the Technical Report ECMA TR/24. It is based on the practical experience of ECMA member companies and the results of their active and continuous participation in the work of ISO, CCITT and various national standardization bodies in Europe and in the USA. It represents a pragmatic and widely based consensus.

The Standard ECMA-103 specifies the Physical Layer of the interface as presented by the data processing equipment. Where appropriate, assumptions of the interface as presented by the private circuit switching network are also indicated.

Accepted as Standard ECMA-103 by the General Assembly of ECMA on June 13, 1985.

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1 Scope and Field of Application

This ECMA Standard defines the Physical Layer characteristics of the basic access interface between data processing equipment (DPE) and private circuit switching networks (PCSN). The interface concerned is at the S reference point as defined in CCITT Recommendation I.411. The reference configuration for the interface is given in Fig. 1.

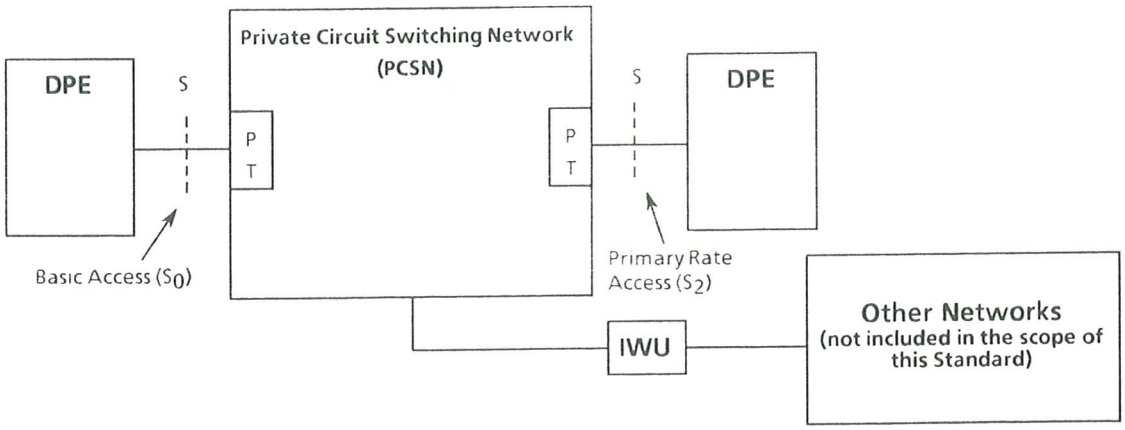


Figure 1 - Reference Configuration for S_0 and S_2 Interfaces

The Standard is based on CCITT Recommendation I.430.

2 References

CCITT Recommendation G.117	Transmission aspects of unbalance about earth (definitions and method)
CCITT Recommendation I.112	Vocabulary of terms for ISDNs
CCITT Recommendation I.320	ISDN protocol reference model
CCITT Recommendation I.411	ISDN user-network interfaces - reference configurations
CCITT Recommendation I.412	ISDN user-network interfaces - interface structures and access capabilities
CCITT Recommendation I.430	Basic user-network interface - layer 1 specification
CCITT Recommendation O.121	Measuring arrangements to assess the degree of unbalance about earth
CCITT Recommendation V.52	Characteristics of distortion and error-rate measuring apparatus for data transmission
CCITT Recommendation V.57	Comprehensive data test set for high data signalling rates
CCITT Recommendation X.200	Reference model of Open Systems Interconnection for CCITT applications
CCITT Recommendation X.211	Physical layer service definitions of open system interconnections for CCITT applications
CCITT Recommendation Z.101..104	Recommendations on the functional specification and description language (SDL)

Note: For the CCITT Recommendations listed above their Red Book versions apply.

ISO 7498	Open Systems Interconnection - Basic Reference Model
ECMA-57	Safety Requirements for Data Processing Equipment

3 Definitions

A basic vocabulary of terms can be found in CCITT Recommendation I.112. In addition, the following definitions apply in this Standard:

B-Channel
The B-channel is a 64 kbit/s access channel with bit and octet timing. It is used to carry user data in both directions of transmission between DPEs connected over a PCSN.

D-Channel
The D-channel is a 16 kbit/s access channel. It is used to carry signalling and other information in both directions of transmission between a DPE and the PCSN.

Data Processing Equipment (DPE)
Specific type of terminal equipment, exclusively or mainly used to process data (in contrast to a voice-only terminal).

Interworking Unit (IWU)
An IWU is the functional block needed for a PCSN to interwork with other networks.

Layer Service
This term is defined in the ISO Reference Model on Open Systems Interconnections (ISO 7498).

Private Circuit Switching Network (PCSN)
An entity providing circuit switching funtions with full digital transmission capability. It is operated by the user and located on his premises to cover the communications needs in his domain. It is bounded by S interfaces.

PCSN Termination (PT)
The termination of a PCSN at the S reference point.

S_0 Interface
The S_0 interface is the basic access interface at the S reference point (see CCITT Recommendation I.411) operating at a physical bit rate of 192 kbit/s. It provides access to two B-channels and one D-channel (2B + D). The S_0 interface forms one of the user access points to a PCSN.

S_2 Interface
The S_2 interface is the primary rate access interface at the S reference point (see CCITT Recommendation I.411) operating at a physical bit rate of 2048 kbit/s. It provides access to 30 B-channels and one D-channel (30B + D). The S_2 interface forms one of the user access points to a PCSN.

Specification and Description Language (SDL)
The specification and description language according to CCITT Recommendations Z.101...Z.104.

Terminal Equipment (TE)
A general term to designate any terminal (voice or data processing or combination of both) connected to a PCSN at the S_0 or at the S_2 interface.

4 Layer Service Characteristics

General information on layer services and layered protocols can be found in CCITT Recommendation X.200 and ISO 7498.

4.1 Layer Services required from the Physical Medium

The Physical Layer of this interface requires a balanced metallic transmission medium for each direction of transmission, capable of supporting 192 kbit/s.

4.2 Layer Services provided to the Data Link Layer

The Physical Layer provides the following layer services to the Data Link Layer:

4.2.1 Transmission capability by means of appropriately encoded bitstreams, for both B-channels and the D-channel.

4.2.2 Timing and synchronization functions.

4.2.3 The signalling capability and the necessary procedures to enable user terminals and/or network terminating equipment to be activated and deactivated. The activation and deactivation procedures are defined in 8.2.

4.2.4 The signalling capability and the necessary procedures to allow terminals to gain access to the common resource of the D-channel in an orderly fashion, while meeting the performance requirements of the D-channel signalling systems. These D-channel access control procedures are defined in 8.1.

4.2.5 The signalling capability and procedures and the necessary functions at the Physical Layer to enable the maintenance functions to be performed.

4.2.6 An indication to the higher layers and the Management Entity about the status of the Physical Layer.

4.3 Primitives between the Physical Layer and other Entities

4.3.1 The primitives used between the Physical Layer and other entities are:

PH-AI/AR, MPH-AI/AR	see 8.2.1.4
PH-DI, MPH-DI/DR	see 8.2.1.5
MPH-EI/ES	see 8.2.1.6
PH-DATA-I/R	PHYSICAL LAYER DATA INDICATION/REQUEST These primitives are used to indicate the arrival of a message unit or to request that a message unit be sent.

4.3.2 The primitives represent the logical exchange of information and control between the Physical Layer, the Data Link Layer and the Management Entity, see Figure 2. They do not specify nor constrain the implementation of entities or interfaces. For a description of the syntax and use of the primitives refer to CCITT Recommendation X.211.

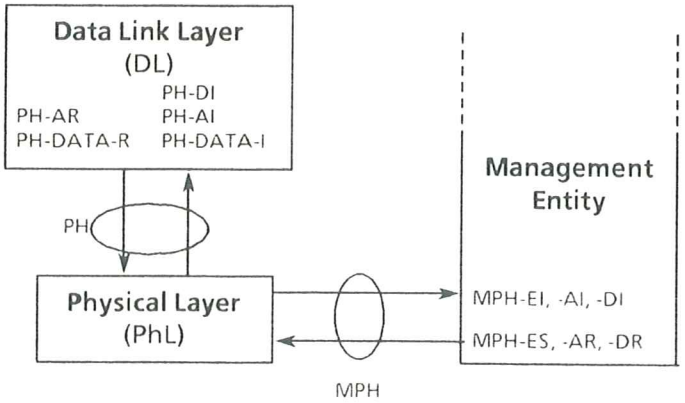


Figure 2 - Physical Layer Primitives

4.3.3 The values of the primitives are defined in Table 1. Relevant detailed description of the primitives and their procedures are given in 8.2.1.

Generic Name	Function			Parameter		Message Unit Contents	
	Request	Indication	Response	Priority Indicator	Message Unit		
PH-DATA	x (Note 1)	x	–	x (Note 2)	x	Data Link Layer peer-to-peer message	↑ between Physical and Data Link Layer ↓
PH-ACTIVATE	x	x	–	–	–		
PH-DEACTIVATE	–	x	–	–	–		↑ between Physical Layer and Management Entity ↓
MPH-ACTIVATE	x	x	–	–	–		
MPH-DEACTIVATE	x	x	x	–	x		
MPH-ERROR	–	x (Note 3)	x (Note 4)	–	x	Additional Information	

Note 1:
PH-DATA-REQUEST implies underlying negotiation between the Physical and the Data Link Layer for the acceptance of the data.
Note 2:
Priority indication applies only to the REQUEST type.
Note 3:
The INDICATION includes the type of the error.
Note 4:
The RESPONSE indicates that search for frames should be abandoned.

Table 1 - Values of Physical Layer Primitives

5 Modes of Operation

The characteristics of the Physical Layer interface allow for point-to-point and point-to-multipoint modes of operation. The mode of operation used at the Physical Layer does not affect the procedures at higher layers.

5.1 Point-to-Point Operation

Point-to-point operation at the Physical Layer implies that only one source (sender) and one sink (receiver) are active at the interface at any one time in each direction of transmission. Such operation is independent of the number of connectors which may be provided on a particular wiring configuration (see Chapter 6).

5.2 Point-to-Multipoint Operation

Point-to-multipoint operation at the Physical Layer allows more than one terminal (source and sink pair) to be simultaneously active at an S reference point. The multipoint mode of operation may be accomodated, as discussed in Chapter 6, with point-to-point or point-to-multipoint wiring configurations.

6 Types of Wiring Configuration

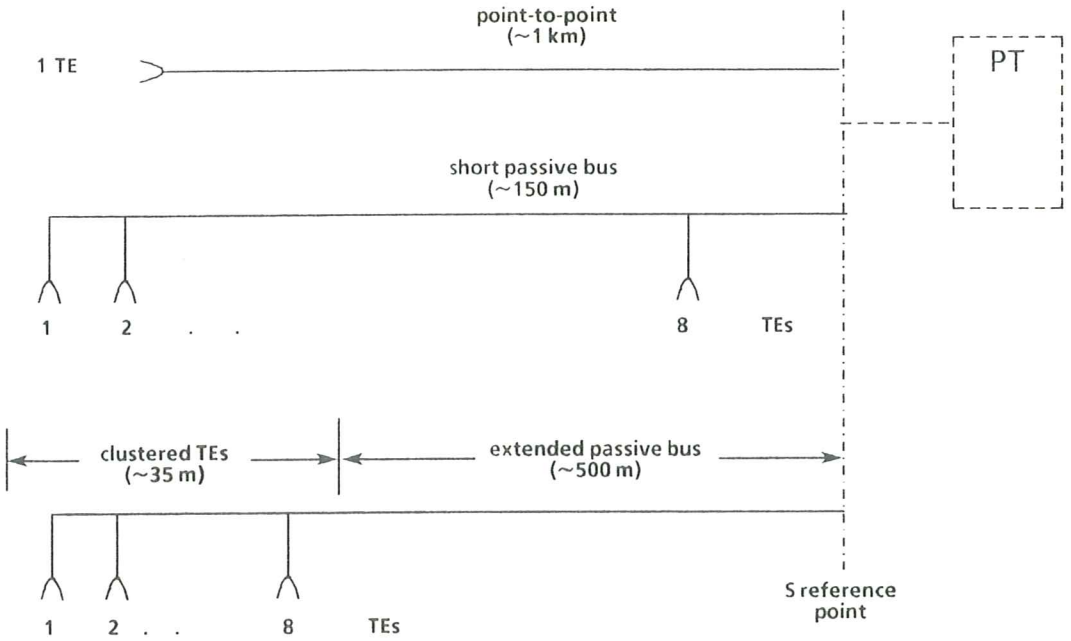
Figure 3 shows general reference configurations for the wiring at user premises. The electrical characteristics of the S_0 interface are determined on the basis of certain assumptions about the various wiring configurations which may exist within users' premises. These assumptions are identified in the configuration descriptions of Figure 3.

6.1 Point-to-Point Configuration

Point-to-point wiring configuration implies that only one source (sender) and one sink (receiver) are interconnected via an interchange circuit.

6.2 Point-to-Multipoint Configuration

Point-to-multipoint wiring configurations allow more than one source to be connected to the same sink or more than one sink to be connected to the same source via an interchange circuit. Such



Note:
The lengths depend on the electrical characteristics of the cabling and the values indicated are given for tutorial background information only.

Figure 3 - Reference Configurations for Basic Access Wiring at the User's Premises

distribution systems are called "passive busses" and are characterized by the fact that they contain no active logic elements.

6.3 Wiring Polarity Integrity

For a point-to-point wiring configuration the two wires of the interchange circuit pair may be reversed. However for point-to-multipoint wiring configurations, the wiring polarity integrity of the interchange circuit from the TEs to the PT must be maintained between the TEs.

6.4 Location of the Interfaces

The wiring on the user's premises is considered to be one continuous cable run with sockets for the TE attached directly to the cable or using stubs of shorter than 1 m in length. The socket and the wiring on the user's premises are beyond the scope of this Standard (see Figure 4).

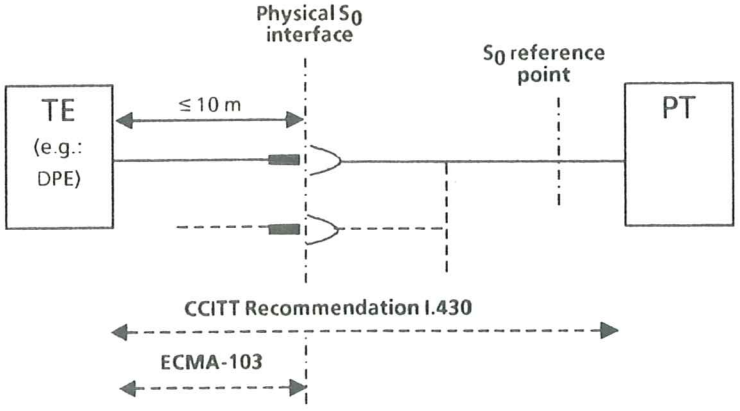


Figure 4 - Location of the S_0 Interface

6.5 DPE Associated Wiring

The wiring between DPE and its associate socket can affect the electrical characteristics of the interface. Thus, a connection cord of not more than 10 m and a plug are considered to form part of the DPE.

7 Functional Characteristics

7.1 Interface Functions

7.1.1 Bit Timing
This function provides bit (signal element) timing at 192 kbit/s to enable DPE and PT to recover information from the aggregate bit stream.

7.1.2 Octet Timing
This function provides 8 kHz octet timing for the PT and DPE.

7.1.3 Frame Alignment
This function provides information to enable PT and DPE to recover the time division multiplexed channels.

7.1.4 B-Channel
This function provides two independent access channels each having a bit rate of 64 kbit/s for each direction of transmission, as defined in CCITT Recommendation I.412.

7.1.5 D-Channel
This function provides an access channel with a bit rate of 16 kbit/s for each direction of transmission, as defined in CCITT Recommendation I.412.

7.1.6 D-Channel Access Control
This function is specified to enable terminals to gain access to the common resource of the D-channel in an orderly controlled fashion. The functions necessary for these procedures include an echoed D-channel at a bit rate of 16 kbit/s in the direction PT to DPE. For the definition of the procedures relating to D-channel access control see 8.1.

7.1.7 Power Feeding
This function provides for the capability to transfer power across the interface from the PCSN (PT) to the DPE. The detailed specification of the power feeding function is given in Chapter 11.

7.1.8 Deactivation
This function is specified in order to permit the DPE to be placed in a lower power consumption mode, eg. when no call is in progress. The procedures and precise conditions under which deactivation takes place are specified in 8.2.

7.1.9 Activation
This function allows DPE and PT to be restored to their normal operating power mode. The procedures and precise conditions under which such deactivation takes place are specified in 8.2.

7.2 Interchange Circuits
Two interchange circuits, one for each direction of transmission, are used to transfer digital signals across the interface. All functions described in 7.1, except for power feeding, shall be carried by means of a digitally multiplexed signal structured as defined in 7.4.

7.3 Connected / Disconnected Indication
The appeareance / disappearance of power is the criterion used by the DPE to determine whether it is connected / disconnected.

A terminal powered across the interface considers itself connected when it detects the presence of power.

A terminal not powered across the interface may consider itself disconnected if it can detect the disappearance of voltage from power source 1 (when provided; see Chapter 11).

The indication, that the terminal is disconnected, is sent to the Management Entity by means of the MPH-Error Indication primitive.

7.4 Frame Structure

In both directions of transmission, the bits are grouped into frames of 48 bits each. The frame structure shall be identical for point-to-point and point-to-multipoint configurations.

7.4.1 Bit Rate

The frame structures are different for each direction of transmission. Both structures are illustrated in Figure 5.

7.4.2 Binary Organization of the Frame

The nominal transmitted bit rate at the interface is 192 kbit/s in both directions of transmission.

7.4.2.1 DPE to PCSN

Each frame consists of the following groups of bits, each individual group being DC-balanced by a trailing bit (L-bit):

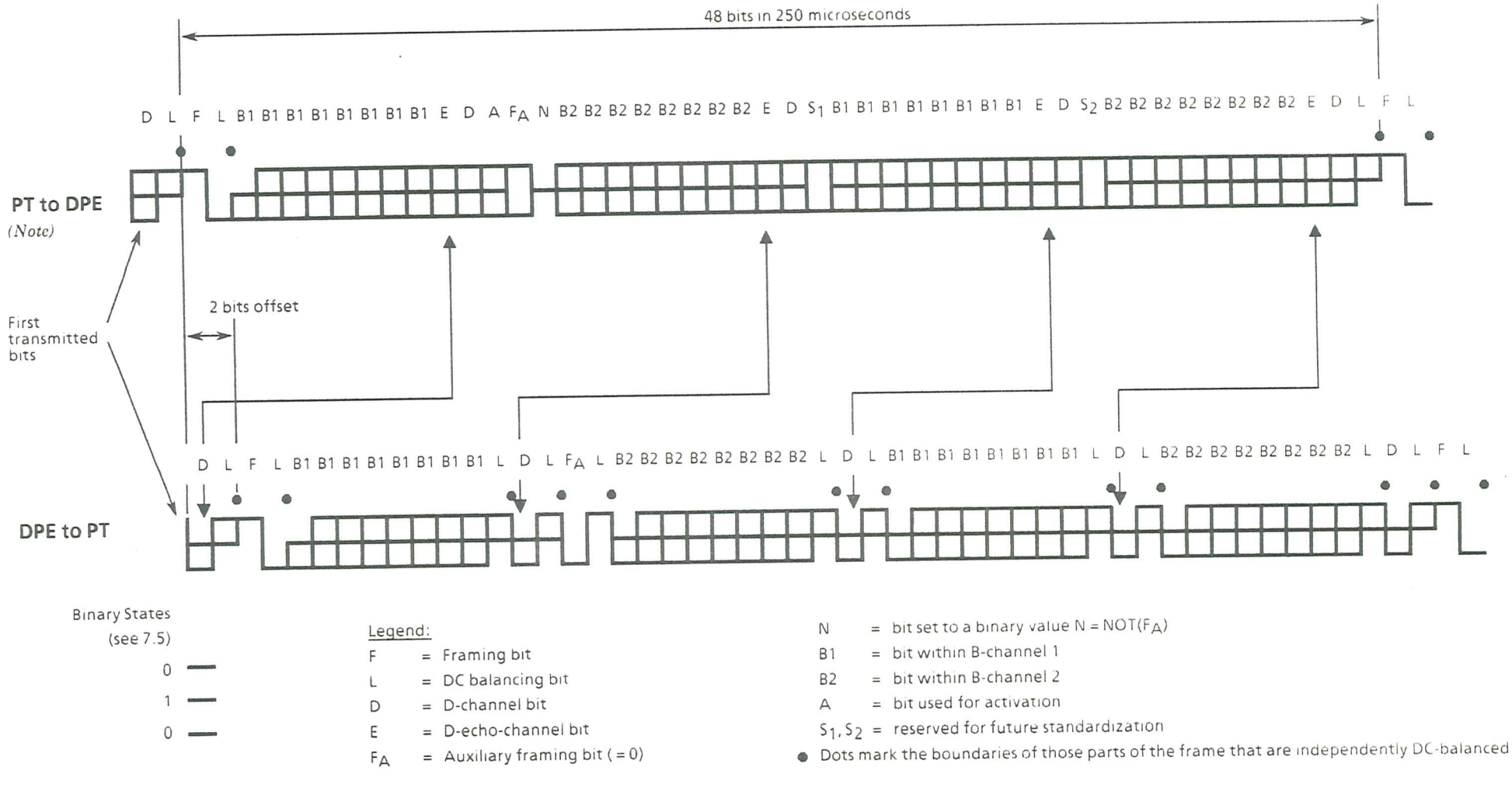
bit position	group
1 and 2	F and L-bit, framing and balance bits
3 to 11	B1-channel with balance bit (first octet)
12 and 13	D and l-bit, D-channel bit with balance bit
14 and 15	F_A and L, auxiliary framing and balance bits
16 to 24	B2-channel with balance bit (first octet)
25 and 26	D and L-bit, D-channel bit with balance bit
27 to 35	B1-channel with balance bit (second octet)
36 and 37	D and L-bit, D-channel bit with balance bit
38 to 46	B2-channel with balance bit (second octet)
47 and 48	D and L-bit, D-channel bit with balance bit

7.4.2.2 PCSN to DPE

Frames transmitted by the PCSN contain a D-echo channel (E-bits) used to re-transmit the D-bits received from the terminals. The D-echo channel is used for D-channel access control. The last bit of the frame (L-bit) is used for balancing each complete frame. The bits are grouped as follows:

bit position	group
1 and 2	F and L-bits, framing and balance bits
3 to 10	B1-channel (first octet)
11	E-bit, D-Echo-channel bit
12	D-channel bit
13	A-bit used for activation
14	F_A-bit, auxiliary framing bit
15	N-bit (coded as defined in Figure 5)
16 to 23	B2-channel (first octet)
24	E-bit, D-Echo-channel bit
25	D-channel bit
26	S_1-bit reserved for future standardization
27 to 34	B1-channel (second octet)
35	E-bit, D-Echo-channel bit
36	D-channel bit
37	S_2-bit reserved for future standardization
38 to 45	B2-channel (second octet)
46	E-bit, D-Echo-channel bit
47	D-channel bit
48	L-bit, frame balance bit

Note:
Pending future standardization, the S_1-bit and the S_2-bit are set to binary ZERO.



Note:
Due to possible reversion of the two wire interchange circuit (see 6.3), the bits may be received with opposite polarity.

Figure 5 - Frame Organization

7.4.2.3 Relative Bit Positions

At the terminals, timing in the direction DPE to PT is derived from the frames received from the PT.

The first bit of each frame transmitted from a DPE towards the PT is offset by two bit periods with respect to the first bit of the frame received from the PT. Figure 5 illustrates the relative bit positions for both transmitted and received frames.

7.5 Line Code

For both directions of transmission pseudo-ternary coding is used with 100% pulse width as shown in Figure 6. Coding is so that a binary ONE is represented by no signal voltage applied to the line whereas a binary ZERO is represented by a positive or negative voltage, ie. a positive or negative pulse.

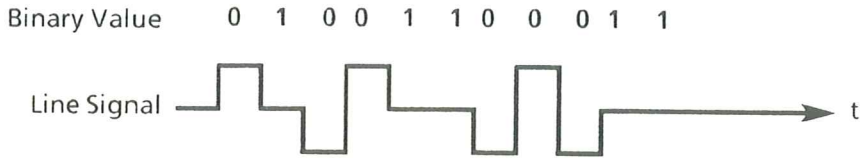


Figure 6 - Pseudo-Ternary Code (Example)

The framing bit (bit 1, "F") is always transmitted as a positive pulse. The balance bit (bit 2, "L") immediately following the framing bit is of opposite polarity.

The first binary ZERO following bit 2 is of the same polarity as bit 2. Subsequent binary ZEROs alternate in polarity. A balance bit is a binary ZERO if the number of binary ZEROs following the last balance bit is odd. It is a binary ONE if the number of binary ZEROs following the last balance bit is even.

Note:
Due to possible reversion of the two wire interchange circuit (see 6.3), the bits may be received with opposite polarity.

7.6 Timing Considerations

A DPE shall synchronize its timing (bit, octet, frame) to the signal received from the PCSN and use this derived timing to synchronize its transmitted signal.

8 Interface Procedures

General Information on interface procedures and layered protocols can be found in CCITT Recommendation X.200 and Standard ISO 7498. The subsequent paragraphs describe the detailed procedures at the Physical Layer interfaces to the Data Link Layer and to the Management Entity.

8.1 D-Channel Access Procedure

The following procedure allows for a number of terminals, being part of a multipoint configuration, to gain access to the D-channel in an orderly fashion. The procedure ensures that, even in cases where two or more terminals attempt to access the D-channel simultaneously, one terminal will always be successful in completing transmission of its information. This procedure relies upon the use of the Data Link Layer frames delimited by flags consisting of the binary pattern 01111110 and the technique of insertion of ZEROs to prevent flag imitation; see Standard ECMA-105.

The D-channel access procedure also permits terminals to operate in a point-to-point manner.

8.1.1 Interframe Time Fill

When a DPE or PT has no Data Link layer frames to transmit, it shall send binary ONEs on the D-Channel.

8.1.2 D-Echo Channel

On receipt of a D-channel bit from the DPE(s), the PT shall reflect its binary value in the next available D-echo channel bit position towards the DPE(s).

8.1.3 D-Channel Monitoring

In the ACTIVATED state (see 8.2) the DPE shall monitor the D-echo channel and count the number of consecutive ONEs. If a ZERO is detected, the terminal shall restart counting the number of consecutive ONEs. The current value of the count is called C. It need not be incremented after the value 11 (decimal number) has been reached.

8.1.4 Priority Mechanism

The Data Link Layer frames are transmitted in such a way that signalling information is given priority (priority class 1) over all other types of information (priority class 2). Furthermore, to ensure that within each priority class all competing DPEs are given a fair chance to access the D-channel, once a DPE has successfully completed the transmission of a frame it is given a lower level of priority within that class. The terminal is given back its normal level within a priority class when all terminals have had an opportunity to transmit information at the normal level within that priority class.

The priority class is passed down from the Data Link Layer as a parameter of the PH-DATA-REQUEST primitive.

The priority mechanism is based on the requirement that a terminal may only start the Data Link Layer frame transmission when C (see 8.1.3) is equal to or exceeds the value X_1 for priority class 1 or is equal to or exceeds the value X_2 for priority class 2. The value X_1 shall be 8 for the normal level and 9 for the lower level of priority. The value X_2 shall be 10 for the normal level and 11 for the lower level of priority.

In either priority class, the value of the normal level of priority is changed into the value of the lower level of priority when a terminal has successfully transmitted a Data Link Layer frame of that priority class.

The value of the lower level of priority is changed back to the value of the normal level of priority when C (see 8.1.3) equals the value of the lower level of priority.

8.1.5 Collision Detection

While transmitting information in the D-channel the terminal shall monitor the received D-echo channel bit and compare the last transmitted bit with the next available D-echo bit. If the transmitted bit is the same as the received echo, the terminal shall continue its transmission. If, however, the received echo is different from the transmitted bit the terminal shall cease transmission immediately and return to the D-channel monitoring state.

8.1.6 SDL Diagram

Figure 7 shows the SDL diagram of the D-channel access procedure. The following variables are used in the SDL diagram:

- C = Count of E-bits received as ONEs
- D = Value of the most recently transmitted D-bit
- i = Priority class of the message to be transmitted (either "1" or "2")
- X_1 = Number of consecutive E-bits to be received as ONEs before transmitting a message of priority class 1
- X_2 = Number of consecutive E-bits to be received as ONEs before transmitting a message of priority class 2
- X_i = Either X_1 or X_2 according to the value of "i"
- Y = Binary variable

The SDL diagram does not cover the queuing functions which are necessary when a second DATA-REQUEST is received before the first message unit has been transmitted.

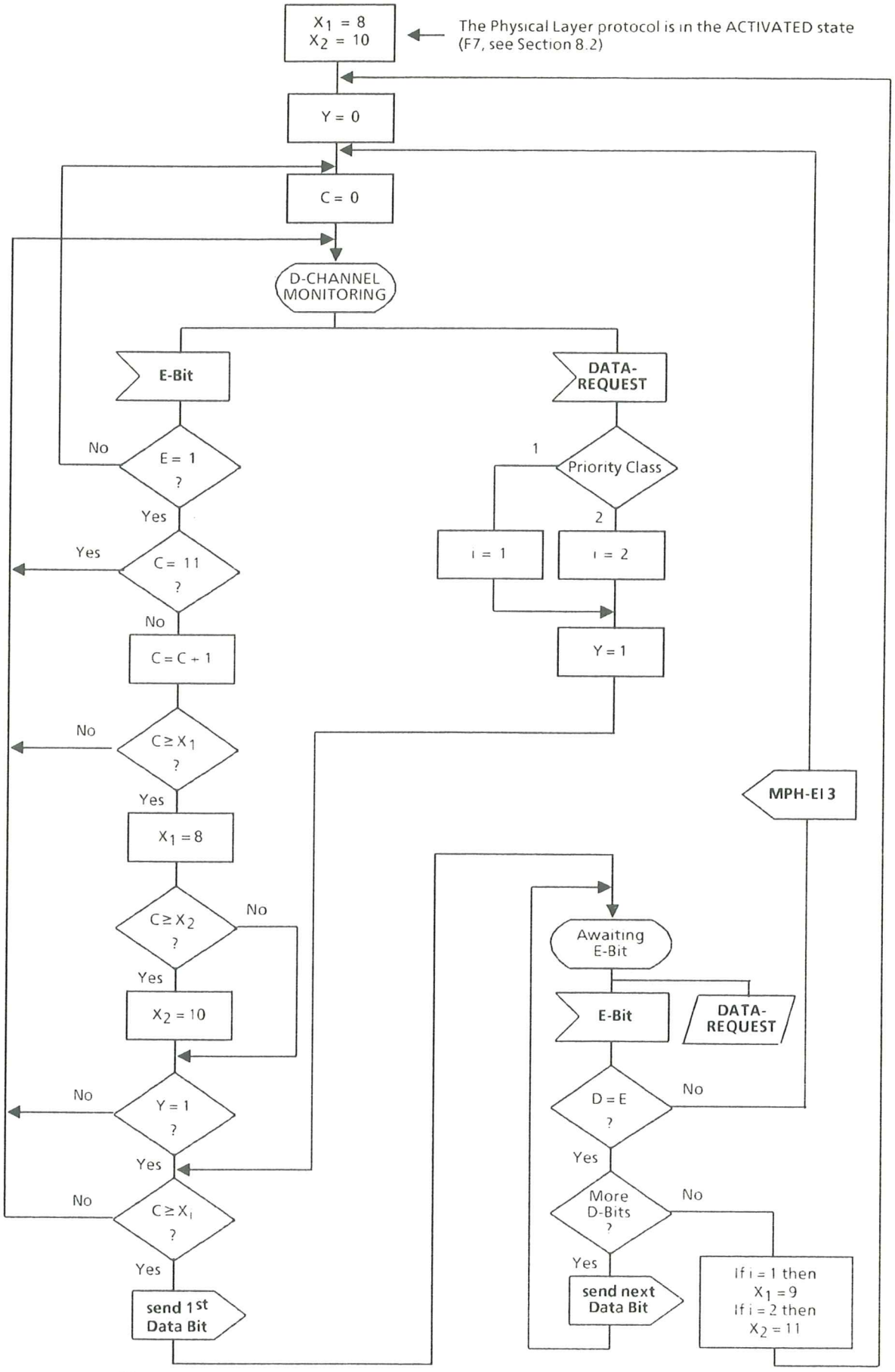


Figure 7 - SDL Presentation of the D-Channel Access Procedure

8.2 Activation / Deactivation

8.2.1 Definitions

8.2.1.1 Signals

The designation, the meaning and the coding of the Physical Layer signals across the S reference point are given in Table 2.

Signals from the PCSN to the DPE		Signals from the DPE to the PCSN	
INFO 0	Transmission of continuous binary ONEs *(Note 1)*; INFO 0 is only recognized by the DPE when it has lasted for longer than 250 µs.	INFO 0	Transmission of continuous binary ONEs *(Note 1)*; INFO 0 is not recognized by the PCSN until it has lasted for longer than 15 ms *(Note 2)*.
		INFO 1	A signal requesting activation, consisting of the continuous transmission of the following pattern: Positive ZERO, negative ZERO, six ONEs Nominal bit rate = 192 kbit/s.
INFO 2	A signal to allow synchronization to the PCSN clock, consisting of frames with all bits of the B-, D- and D-Echo channels, set to binary ZERO, the A-bit set to ZERO, the N- and L-bits set according to the normal coding rules.		
		INFO 3	A signal indicating the SYNCHRONIZED or the ACTIVATED state, consiting of synchronized frames with operational data on the B- and D-channels.
INFO 4	A signal indicating the ACTIVATED state, consisting of frames with operational data on the B- D- and D-echo channels; the A-bit is set to ONE.		

Note 1:
For the coding of binary ONEs and ZEROs see 7.5.

Note 2:
This value ensures that the PCSN remains in the ACTIVATED state while the DPE is recovering from the LOST FRAMING state.

Table 2 - Definition of Physical Layer Signals

8.2.1.2 DPE Side States

F1	POWER OFF	: The DPE is not powered on.
F2	SENSING	: The DPE is powered on, but has not determined the type of signal (if any) that it is receiving.
F3	DEACTIVATED	: The DPE is in the idle state, ie. it is neither transmitting nor receiving a signal.
F4	PENDING ACTIVATION	: When a DPE is requested to initiate activation it transmits INFO 1 and waits for a response from the PCSN.
F5	UNSYN-CHRONIZED	: At the first receipt of any signal from the PCSN, the DPE ceases to transmit INFO 1 and tries to identify signal INFO 2 or INFO 4.
F6	SYNCHRON-IZED	: When the DPE receives the synchronization signal from the PCSN (INFO 2), it responds with INFO 3, indicating that it is in the SYNCHRONIZED state, and waits for normal frames from the PCSN (INFO 4).
F7	ACTIVATED	: This is the normal active state with the protocol activated in both directions. Both the PCSN and the DPE are transmitting frames.
F8	LOST FRAMING	: This is the condition when the DPE has lost frame alignment (see 8.3.1) and is awaiting resynchronization by receipt of INFO 2 or INFO 4 or deactivation by receipt of INFO 0.

8.2.1.3 PCSN Side States

G1	DEACTIVE	: The PT is in the idle state, ie. it is neither transmitting nor receiving a signal.
G2	PENDING ACTIVATION	: When a PT is requested to initiate activation it transmits INFO 2 and waits for a response from the DPE.
G3	ACTIVE	: The normal active state where the PCSN to DPE direction is active. The DPE to PCSN direction may or may no longer be active, ie. the PCSN may deactivate or maintain the ACTIVATED state if the DPE stops transmitting. (The choice to deactivate is completely up to higher layer protocols within the PCSN.)
G4	PENDING DEACTIVATION	: When the PCSN wishes to deactivate it may wait for a timer (T2) to expire before returning to the DEACTIVE state.

8.2.1.4 Activate Primitives

The following primitives are used in the activate procedures:

PH-AR MPH-AR	ACTIVATE REQUEST	: These primitives are used to request that the Physical Layer should be activated.
PH-AI MPH-AI	ACTIVATE INDICATION	: These primitives are used by the Physical Layer to indicate that it has been activated.

8.2.1.5 Deactivate Primitives

The following primitives are used in the deactivate procedures:

MPH-DR	DEACTIVATE REQUEST	: This primitive is used by the Management Entity to request that the Physical Layer should be deactivated.
PH-DI MPH-DI	PH-DEACTIVATE INDICATION	: These primitives are used by the Physical Layer to indicate that it has been deactivated.

8.2.1.6 Error and Recovery Primitives

The following primitives should be used between the Physical Layer and the Management Entity:

MPH-EI	MPH-ERROR INDICATION	: This primitive includes the parameters "1", "2" and "3": MPH-EI 1 indicates an error report. The message unit contains the type of the error. This can be *receiving INFO 2 instead of INFO 4;* *loss of framing;* *power-off information.* MPH-EI 2 reports that no error condition now exists. This can be due to: *power-on.* MPH-EI 3 indicates to the Management Entity that the E-bit received was not equal to the corresponding D-bit. Optional parameters may convey additional information, see 9.3.
MPH-ES	MPH-ERROR RESPONSE	: This primitive indicates that the Physical Layer should abandon further search for framing.

8.2.2 Activation / Deactivation Procedure at the Terminal Side

This procedure is shown in Table 3 in the form of a finite state matrix. A functional SDL description of the procedure is presented in 8.2.5.

State Name	POWER OFF	SENSING	DEACTI-VATED	PENDING ACTIVAT-ION	UNSYN-CHRO-NIZED	SYN-CHRO-NIZED	ACTIVI-VATED	LOST FRAMING
State Number	F1	F2	F3	F4	F5	F6	F7	F8
Info sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
power switched off	/	MPH-EI1; F1	MPH-EI1; F1	MPH-EI1; F1	MPH-EI1; F1	MPH-EI1; F1	MPH-EI1; F1	MPH-EI1; F1
power switched on	MPH-EI2; F2	/	/	/	/	/	/	/
MPH-Activate Request	/	–	set T3 *(Note 1)*; F4	–	–	–	(M)PH-AI	–
Expiry of Timer T3 *(Note 1)*	/	–	–	(M)PH-DI; F3	(M)PH-DI; F3	(M)PH-DI; F3	–	–
Receiving INFO 0	/	F3	–	–	–	(M)PH-DI; MPH-EI2; F3	(M)PH-DI; F3	(M)PH-DI; MPH-EI2; F3
Receiving any signal *(Note 2)*	/	–	–	F5	–	/	/	–
Receiving INFO 2	/	F6	F6	/	F6	–	MPH-EI1; F6	F6
Receiving INFO 4	/	(M)PH-AI; F7	(M)PH-AI; F7	/	(M)PH-AI; F7	(M)PH-AI; MPH-EI2; F7	–	(M)PH-AI; MPH-EI2 ; F7
Lost Framing	/	/	/	/	/	MPH-EI1; F8	MPH-EI1; F8	–
MPH-Error Response	/	–	–	–	–	–	–	(M)PH-DI; F3

Legend: – No Change
/ Impossible Situation
P;Fn means: "Issue primitive P and then go to state Fn"
Primitives: According to 8.2.1.5, MPH-EI includes parameters "1" or "2" indicating the report of an error or the report of recovery, respectively.

Note 1:
Timer T3 may be implemented in the Physical Layer or elsewhere.
Note 2:
This event reflects the case where some signal is received and the DPE has not (yet) determined whether it is INFO 2 or INFO 4.

Table 3 - Finite State Matrix on the Activation / Deactivation Procedure of the Physical Layer at the DPE Side

8.2.3 Activation / Deactivation Procedure at the PCSN Side

This procedure is beyond the scope of this Standard. For the provision of background information, however, it is shown in Table 4 in the form of a finite state matrix. A functional SDL description of the procedure is presented in 8.2.5.

8.2.4 SDL Presentation of the Activation / Deactivation Procedure

Figures 8 to 19 show the interworking between the DPE and (as far as applicable and necessary for understanding) the PCSN side of the Physical Layer Activation/Deactivation protocol. The protocol is partitioned as follows:

Transition from the POWER-OFF to the DEACTIVATED State
The DPE is forced to re-enter the SYNCHRONIZED state
Activation initated by the DPE
Activation Failure at the DPE / PCSN side
Status Verifications
The DPE / PCSN has lost Framing
The DPE has lost Power
The PCSN releases the Physical Layer Connection
Activation initated by the PCSN

State Name	DEACTIVE	PENDING ACTIVATION	ACTIVE	PENDING DE-ACTIVATION
State Number	G1	G2	G3	G4
Info sent	INFO 0	INFO 2	INFO 4	INFO 0
(M)PH-Activate Request	set T1; *(Note 1)* G2	/	(M)PH-AI	set T1; *(Note 1)* G2
(M)PH-Deactivate Request	MPH-DI	set T2; *(Note 2)* G4	set T2; *(Note 2)* G4	–
Expiry of Timer T1 *(Note 1)*	–	set T2; *(Note 2)* (M)PH-DI; G4	–	–
Expiry of Timer T2 *(Note 2)*	–	–	–	(M)PH-DI; G1
Receiving INFO 0	–	–	set T2; *(Note 2)* G4 *(Note 3)*	(M)PH-DI; G1
Receiving INFO 1	set T1; *(Note 1)* G2	–	/	–
Receiving INFO 3	/	(M)PH-AI; G3	–	–
Loss of framing	/	/	set T2; *(Note 2)* G4 *(Note 3)*	–

Legend: – No Change
/ Impossible Situation
P;Gn means: "Issue primitive P and then go to state Gn"

Note 1:
Timer T1 is a supervisory timer which has to take into account the overall time to activate.
Note 2:
Timer T2 prevents unintentional reactivation. Its value is between 25 ms and 100 ms. This implies that a DPE has to recognize INFO 0 and to react on it whithin 25 ms. If the PCSN is able to unambiguously recognize INFO 1, then the value of timer T2 may be 0.
Note 3:
Whether state G4 has to be entered and INFO 0 has to be transmitted, is a function of the specific PCSN.

Table 4 - Finite State Matrix on the Activation / Deactivation Procedure of the Physical Layer at the PCSN Side

The activation/deactivation signals are continuous signals. An (external) output symbol indicates that the transmission of such continuous signal is to be started. The transmission of this signal ends when it is replaced by another signal to be sent in the same direction. An (external) input symbol indicates that an incoming signal has arrived.

The SDL symboling used assumes that the DPE is on the left and the PCSN is on the right hand side of a functional interworking model as depicted in Figure 8:

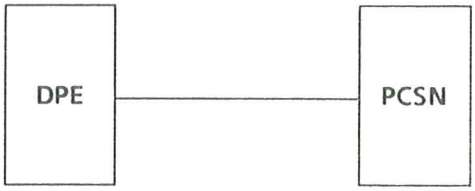
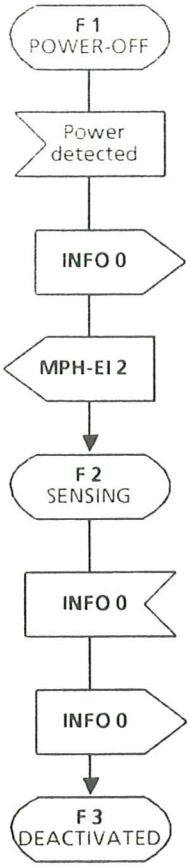
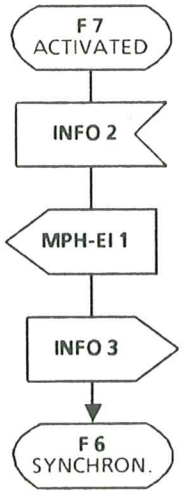


Figure 8 - Functional Interworking Model



There is no corresponding sequence at the PCSN side of the S_0 interface.

Figure 9 - Transition from the POWER-OFF to the DEACTIVATED State



The corresponding sequence at the PCSN side of the S_0 interface is out of the scope of this Standard.

Figure 10 - The DPE is forced to re-enter the SYNCHRONIZED State

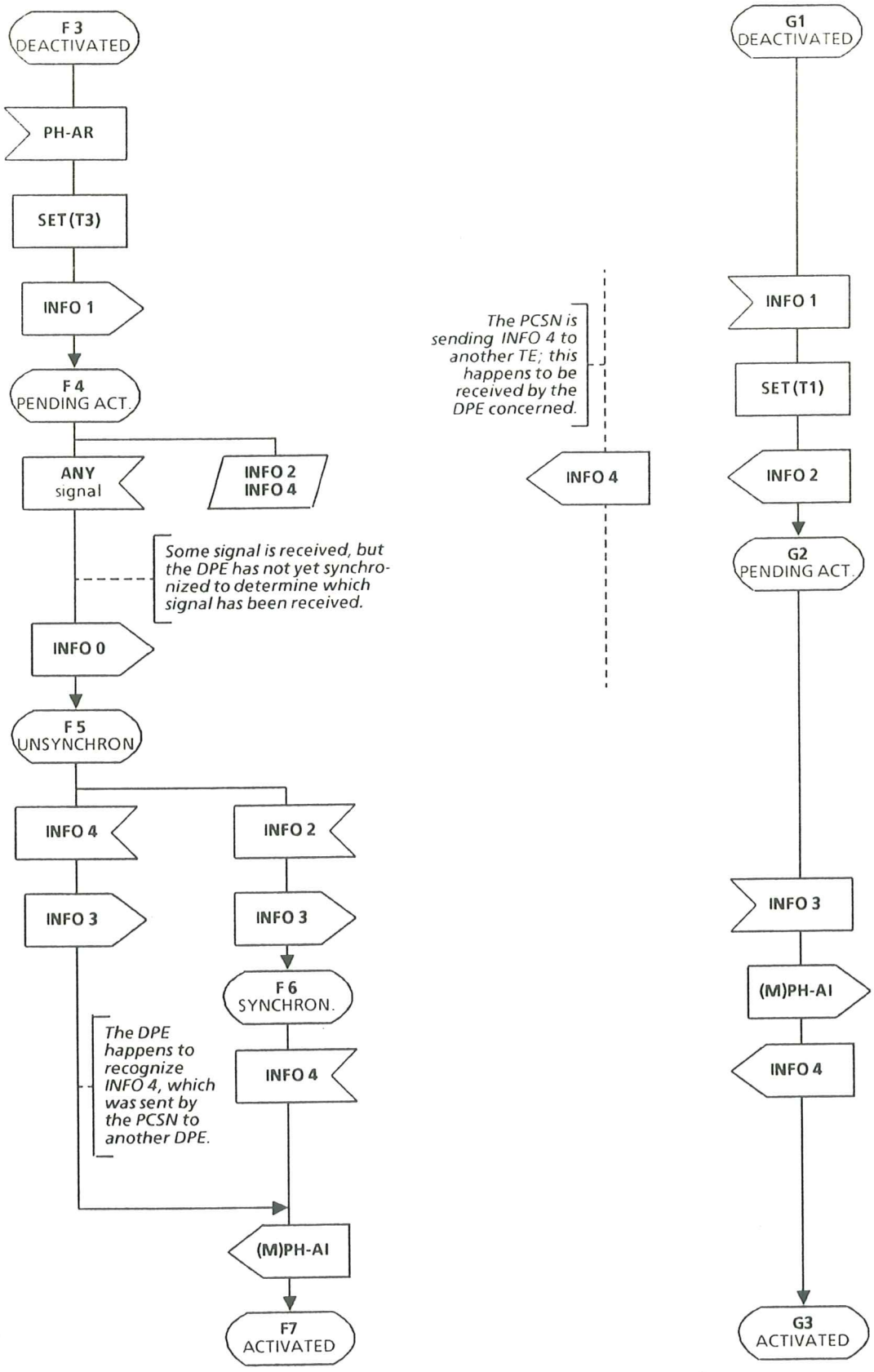


Figure 11 - Activation initiated by the DPE

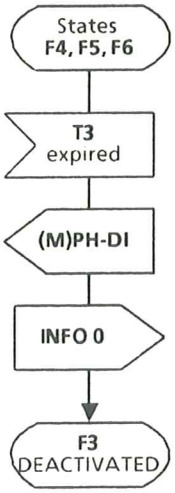


Figure 12 - Activation Failure at the DPE Side

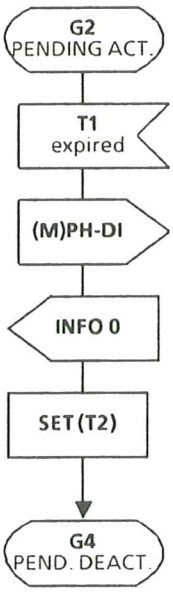
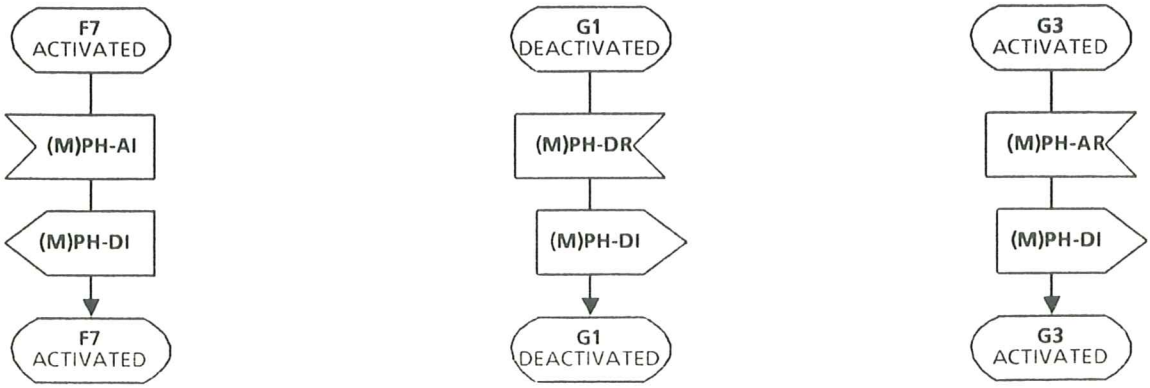


Figure 13 - Activation Failure at the PCSN Side



Figures 14a, b, c - Status Verifications

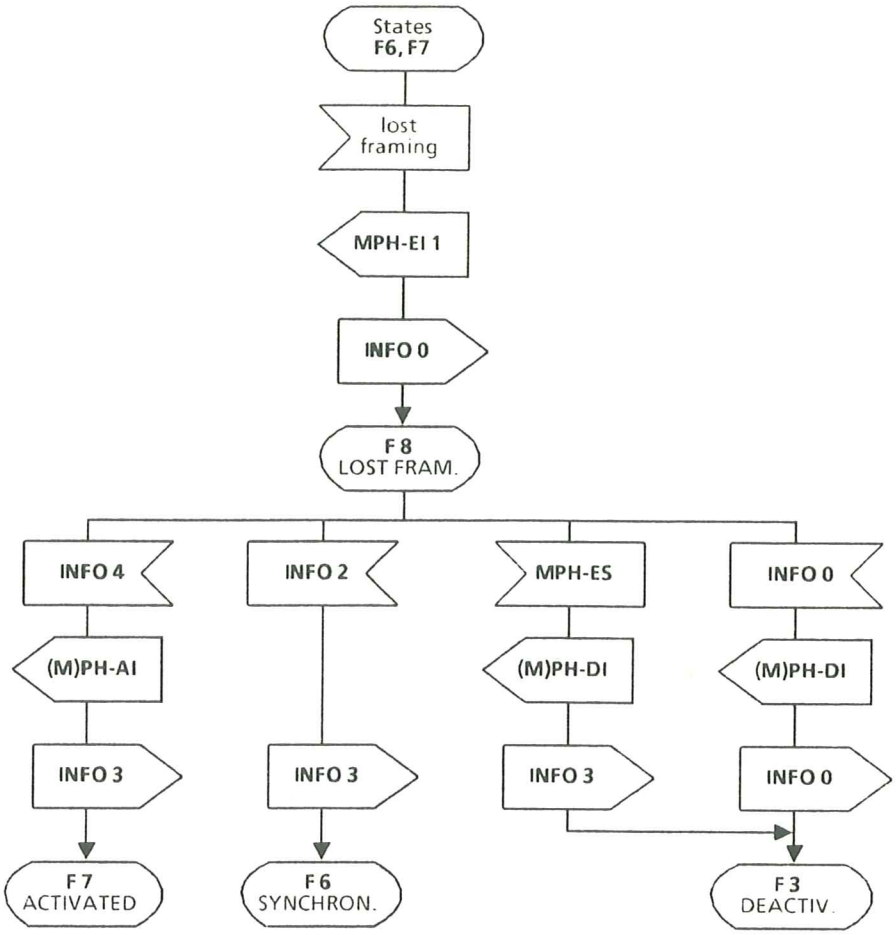


Figure 15 - The DPE has lost Framing

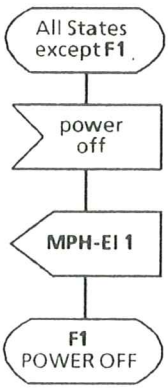
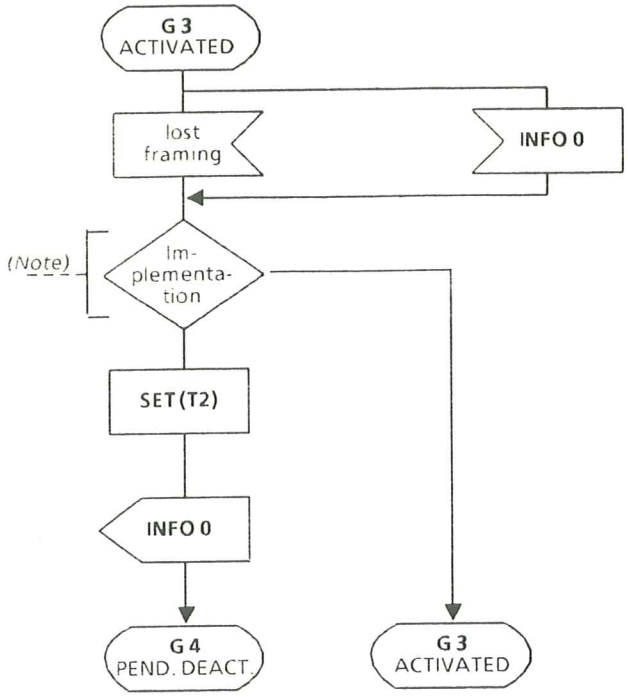


Figure 16 - The DPE has lost Power



Note:
Whether state G4 has to be entered and INFO 0 has to be transmitted, is a function of the specific PCSN.

Figure 17 - The PCSN has lost its Framing

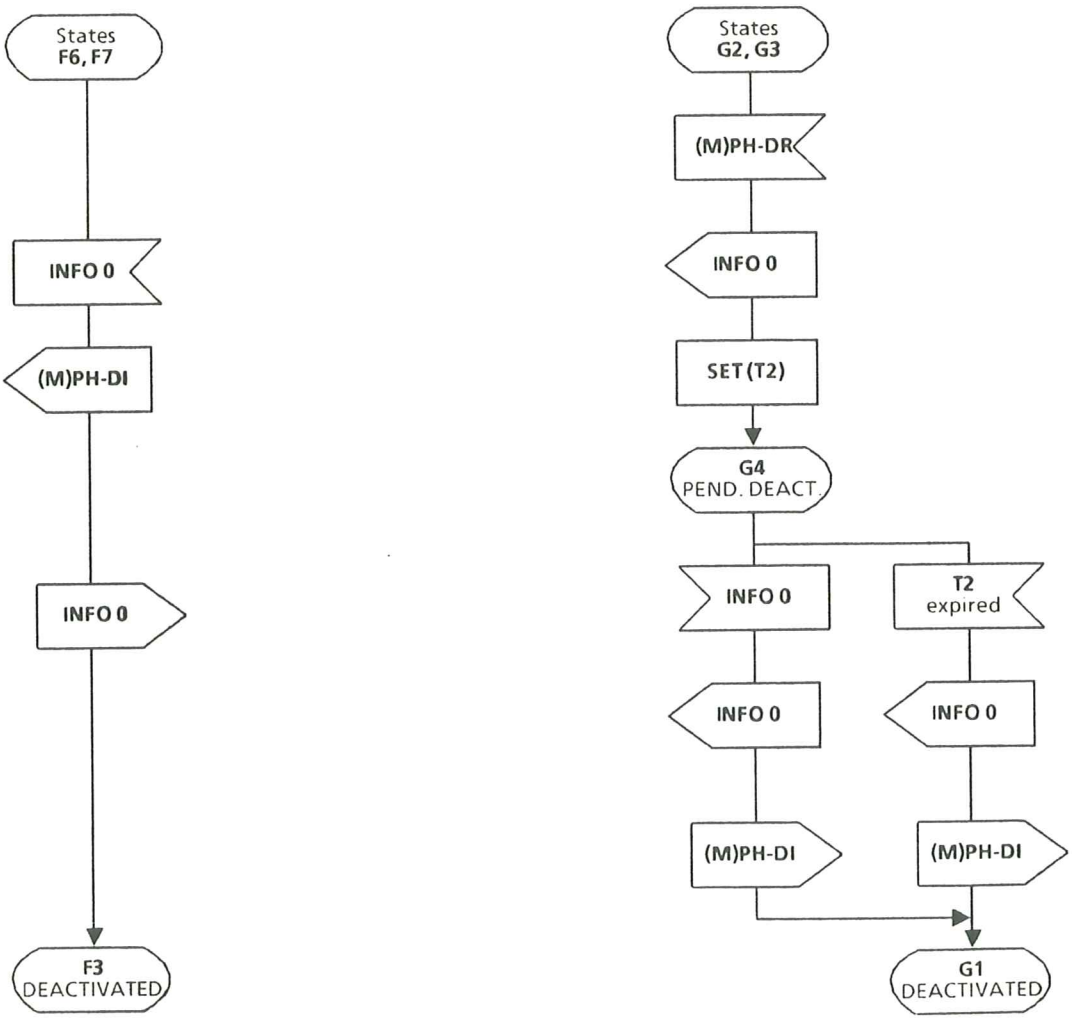


Figure 18 - The PCSN Releases the Physical Layer Connection

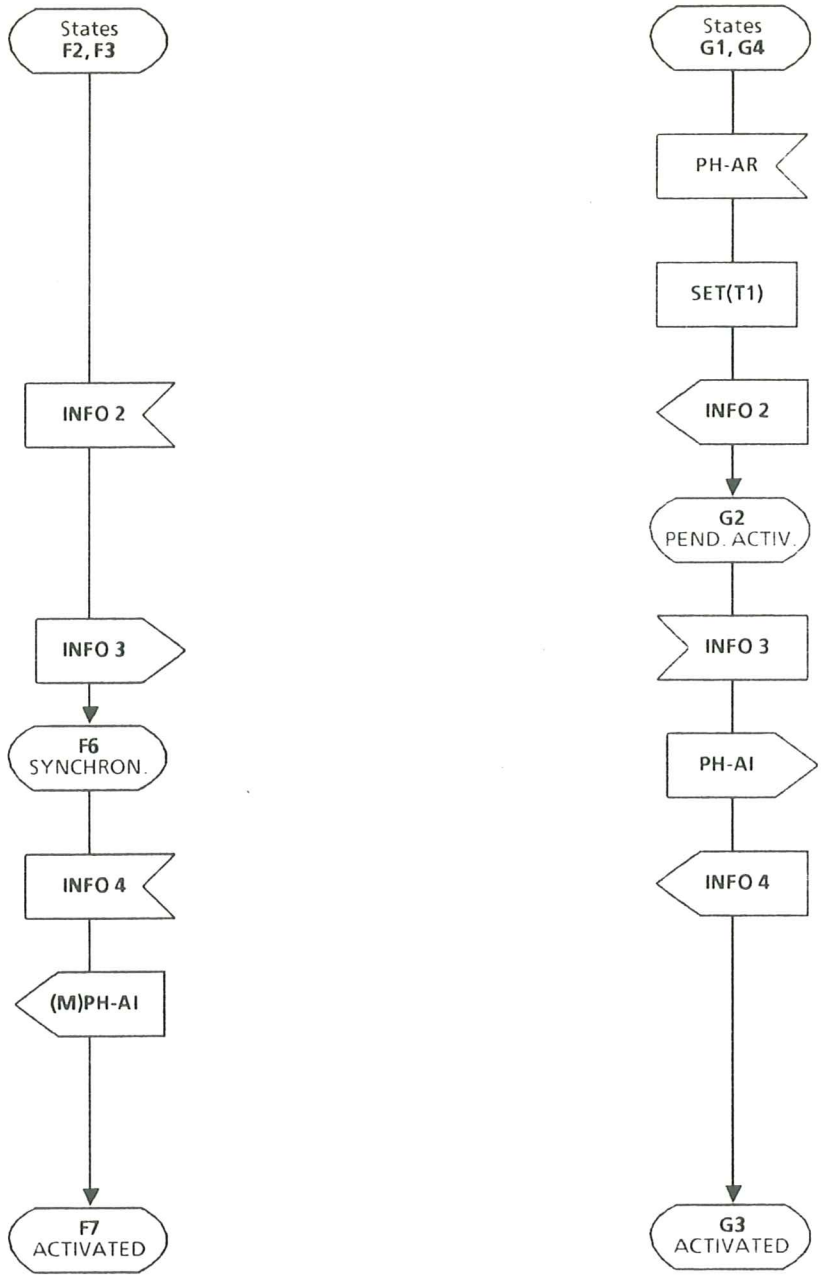


Figure 19 - Activation initiated by the PCSN

8.2.5 Timing Values

8.2.5.1 Timers

The expiry of timers is used to select an alternative sequence in order to continue and conclude the procedure in an orderly fashion even when an expected reaction fails.

Three timers are used in the Physical Layer protocol:

PCSN side: Timer T1 supervizes whether or not the Physical Layer can be activated by the PCSN. The specification of its value is outside the scope of this Standard.
Timer T2 gives the TEs sufficient time to recognize INFO 0 and to enter the DEACTIVATED state. For its value see CCITT Recommendation I.430.

DPE side: Timer T3 gives the PCSN sufficient time to recognize INFO 1 and to respond by transmitting INFO 2. The value of T3 shall be 3 s.
If the PCSN fails to respond before T3 expires, a reattempt may be initiated by higher layers or the Management Entity.

8.2.5.2 Reaction Times of the DPE

In the SYNCHRONIZED state the DPE shall recognize the receipt of INFO 4 within two frames (in the absence of errors).

The DPE shall send INFO 3 within 100 ms of receipt of INFO 2 or INFO 4.

In accordance with CCITT recommendation I.430, the DPE shall react on INFO 0 within 25 ms.

8.3 Frame Alignment Procedures

The frame alignment procedures make use of the fact that the framing bit is represented by a pulse having the same polarity as the preceding pulse (AMI violation); this allows rapid reframing.

According to the coding rule, both the framing bit and the first binary ZERO following the framing balance bit (in the same frame) produce an AMI violation. To guarantee secure framing the auxiliary framing bit pair F_A and N in the direction PT to DPE or the auxiliary framing bit F_A with the associated balancing bit L in the direction DPE to PT are introduced. For the direction PT to DPE, this ensures that there is always an AMI violation at 14 bits or less (the *14 -bit criterion*) from the framing bit F, due to F_A or N being a binary ZERO. For the direction DPE to PT, it ensures that there is always an AMI violation at 13 bits or less (the *13-bit criterion*), due to F_A being always binary ZERO. The framing procedures do not depend on the polarity of the framing bit F and thus are not sensitive to wiring polarity.

The coding rule for the auxiliary framing bit pair F_A and N in the direction PT to DPE is such that N is the binary opposite of F_A, ie. $N = NOT(F_A)$. The F_A and L bit in the direction DPE to PT are always coded such that the binary values of F_A and L are equal.

8.3.1 Frame Alignment Procedure in the Direction PT to DPE

Frame alignment on initial activation of the DPE shall comply with the timing value defined in Section 8.2.6.2.

8.3.1.1 Loss of frame alignment shall be assumed when a time period equivalent to two 48-bit frames has elapsed without having detected valid pairs of AMI violations, obeying the 14-bit criterion as described above. The DPE shall cease transmission immediately.

8.3.1.2 Frame realignment shall be assumed to occur when 3 consecutive pairs of line AMI violations, obeying the 14-bit criterion, have been detected.

8.3.2 Frame Alignment in the Direction DPE to PT

The 13-bit criterion applies.

8.3.2.1 The PT may assume loss of frame alignment if a time period equivalent to two 48-bit frames has elapsed since detecting consecutive violations according to the 13-bit criterion. On detection of loss of framing, the PT may continue transmitting towards the DPE (ie. remain in the ACTIVATED state) or may initiate deactivation by transmitting INFO 0 (ie. take the PENDING DEACTIVATION state).

8.3.2.2 The PT may assume that frame alignment has been regained when 3 consecutive pairs of AMI violations, obeying the 13-bit criterion, have been detected

8.4 Idle Channel Code on B-Channels

A DPE shall send binary ONEs in any B-channel which is not assigned to it. This is the responsibility of higher layers.

9 Provisions for Physical Layer Maintenance

The Physical Layer shall provide the following maintenance facilities:

9.1 Test Loops

Two test loops, Loop A4 and Loop B4, can be activated, see Figure 20.

Loop A4 provides a loop back of both B-channels independently towards the PCSN. The loop shall preserve octet integrity. It shall reflect any bit pattern received at the earliest point of time, ie. with a delay of 2 bits (see 7.4).

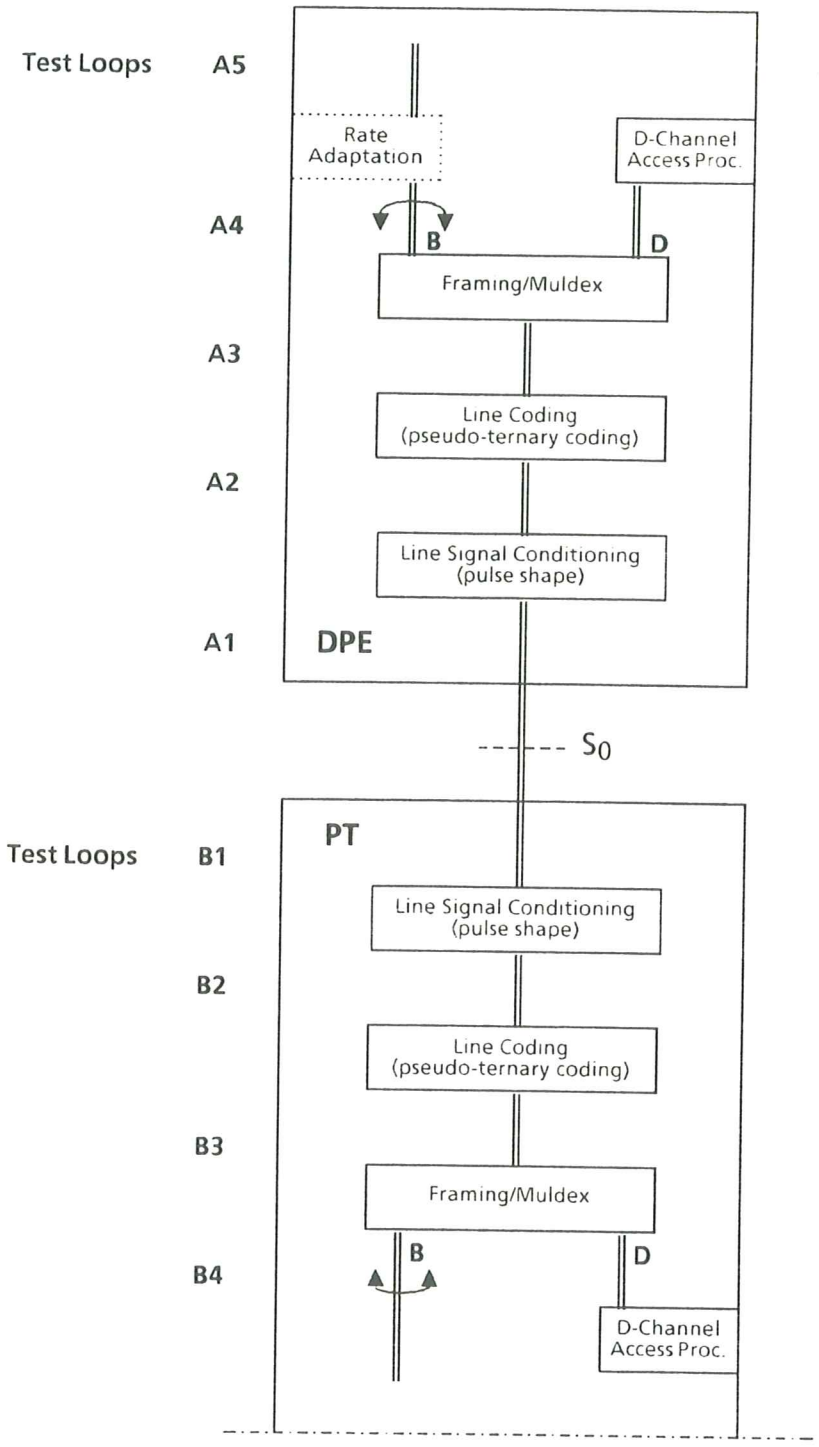


Figure 20 - DPE and PCSN (PT) Test Loops

Loop B4 Whether or not Loop B4 is provided depends on the implementation of the specific PCSN. When provided, it shall loop back both B-channels independently towards the DPE. The DPE will see a delay of 22 bits of any bit pattern applied to the S_0 interface.

9.2 Management Entity Primitives

The test loops shall be activated and deactivated by the Management Entity by means of the primitives:

MPH-LAR	MPH-LOOP ACTIVATION REQUEST	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.
MPH-LDR	MPH-LOOP DEACTIVATION REQUEST	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.

The activated or deactivated state of the loop(s) shall be indicated to the Management Entity by means of the primitives:

MPH-LAI	MPH-LOOP ACTIVATION INDICATION	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.
MPH-LDI	MPH-LOOP DEACTIVATION INDICATION	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.

9.3 Test Bit Stream

9.3.1 Continuous Binary ZEROs

The DPE shall provide the facility to transmit a continuous bit stream consisting of binary ZEROs. This facility shall not be activated or deactivated via the S_0 interface. The PCSN may also provide the facility to transmit a continuous bit stream consisting of binary ZEROs. For the use of the continuous binary ZEROs bit stream see 10.5.6.2.

9.3.2 Isolated Binary ZEROs

In the SYNCHRONIZED state the DPE shall provide the facility to transmit a bit pattern coded 11110111 on both B-channels. The isolated binary ZEROs bit stream shall be used to measure the pulse shapes of the output signal, see 10.5.3.

9.4 D-Echo-Bit

When the E-bit differs from the corresponding D-bit, the MPH-EI 3 primitive shall be sent to the Management Entity. Distinction between bit errors and access collisions (see 8.1.5) by the Management Entity is possible if additional information is conveyed by optional parameters of the primitive (ie. the bit position of the error and the contents of the associated PH-DATA-REQUEST).

10 Electrical Characteristics

From the view point of their electrical characteristics, connection cords and plugs are considered to be part of the DPE.

10.1 Bit Rate

The nominal bit rate at the S_0 interface shall be 192 kbit/s in both directions of transmission, with a tolerance of not more than ± 100 ppm in the free running mode.

10.2 Jitter and bit phase relationship between DPE Input and Ouput

10.2.1 Test Configuration

The jitter and phase deviation measurements are carried out with four different wave forms at the terminal input, in accordance with the following configurations:

I	Point-to-point configuration with 6 dB attenuation measured between the two termination resistors at 96 kHz (high-capacitance cable);
II	Short passive bus with 8 terminals (including the terminal under test clustered at the far end from the signal source; high-capacitance cable);
IIIa, IIIb	Short passive bus with the terminal under test adjacent to the signal source (high and low capacitance cable);
IV	Ideal test signal condition, with the source connected directly to the receiver of the terminal under test (ie. without artificial line).

Examples for wave forms that correspond to the configurations I, II, IIIa and IIIb are given in Figures 21 to 24. Test configurations which can generate these signals are given in Figure 25.

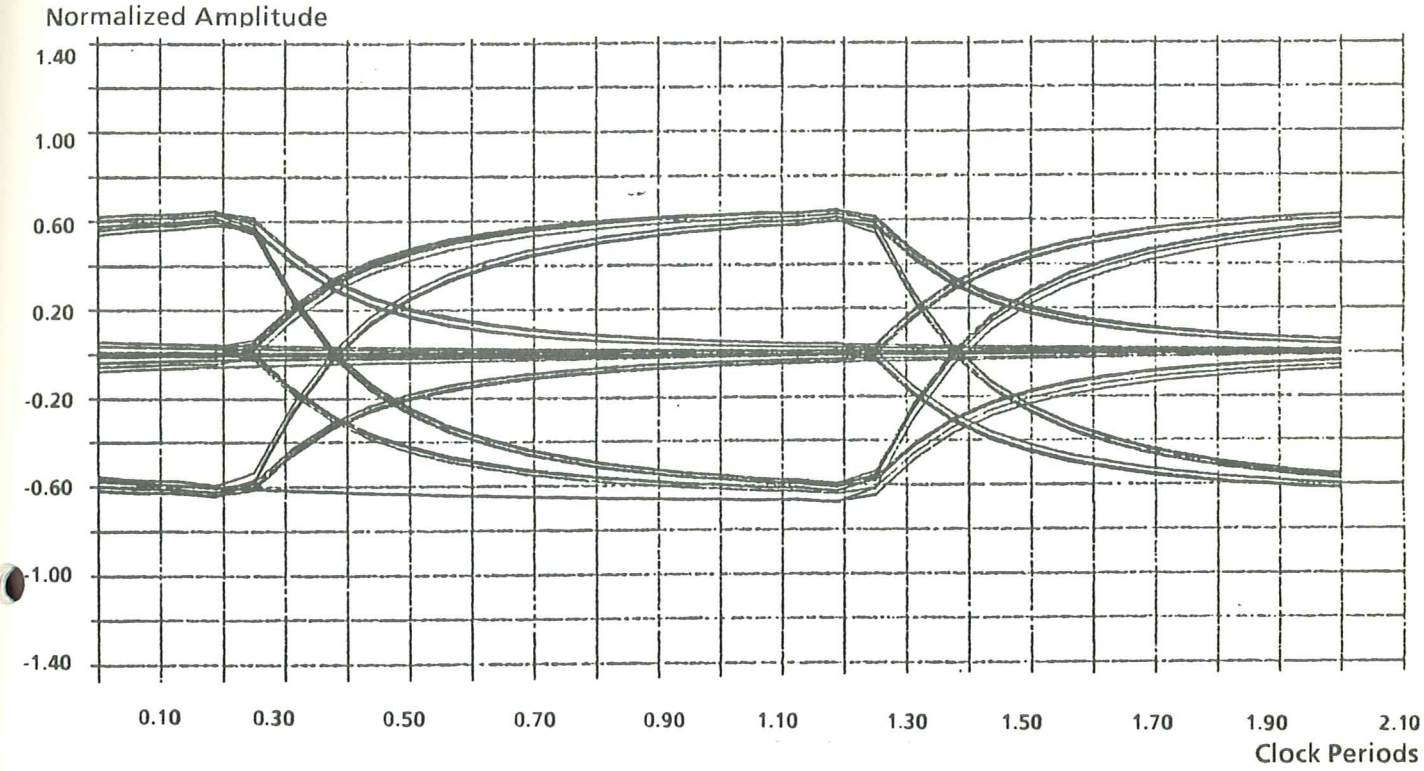


Figure 21 - Waveform of Test Configuration I :
Point-to-Point
(C = 120 nF/km)

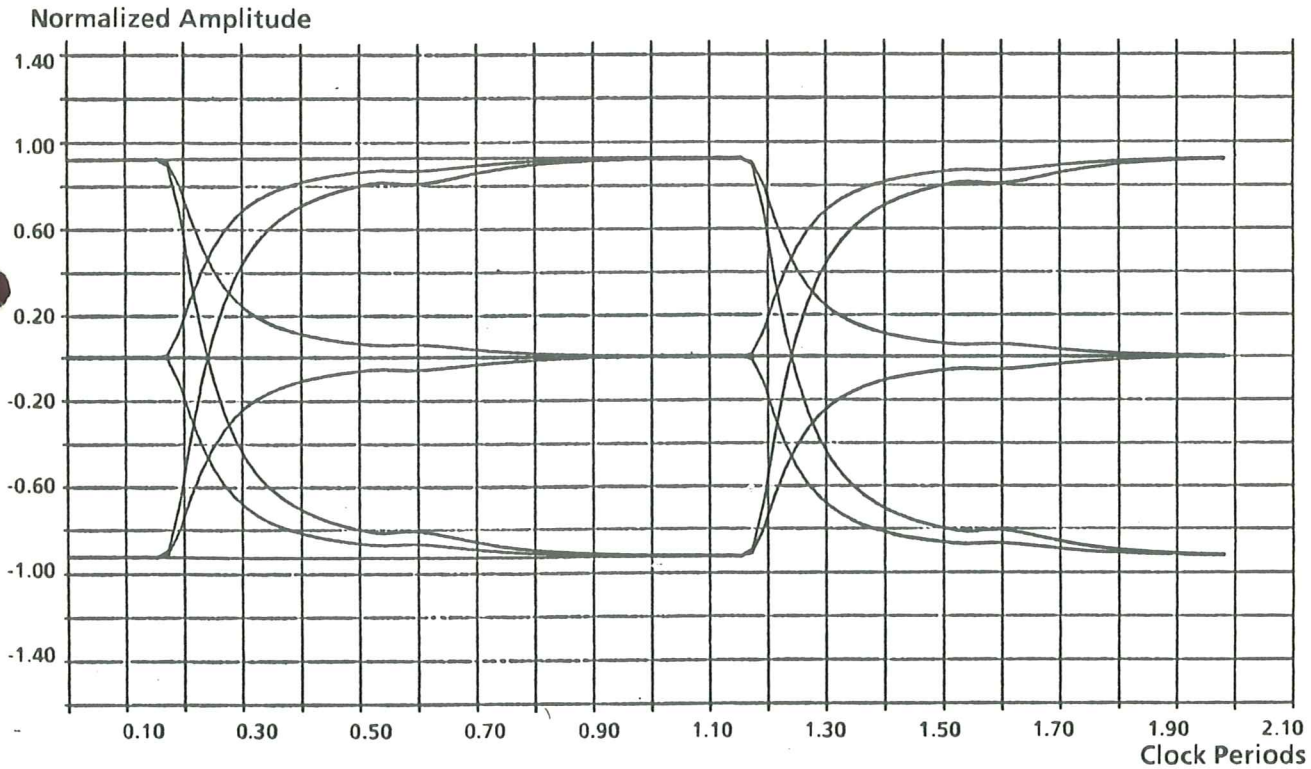


Figure 22 - Waveform of Test Configuration II :
Short Passive Bus with 8 clustered TEs at the far End
(C = 120 nF/km)

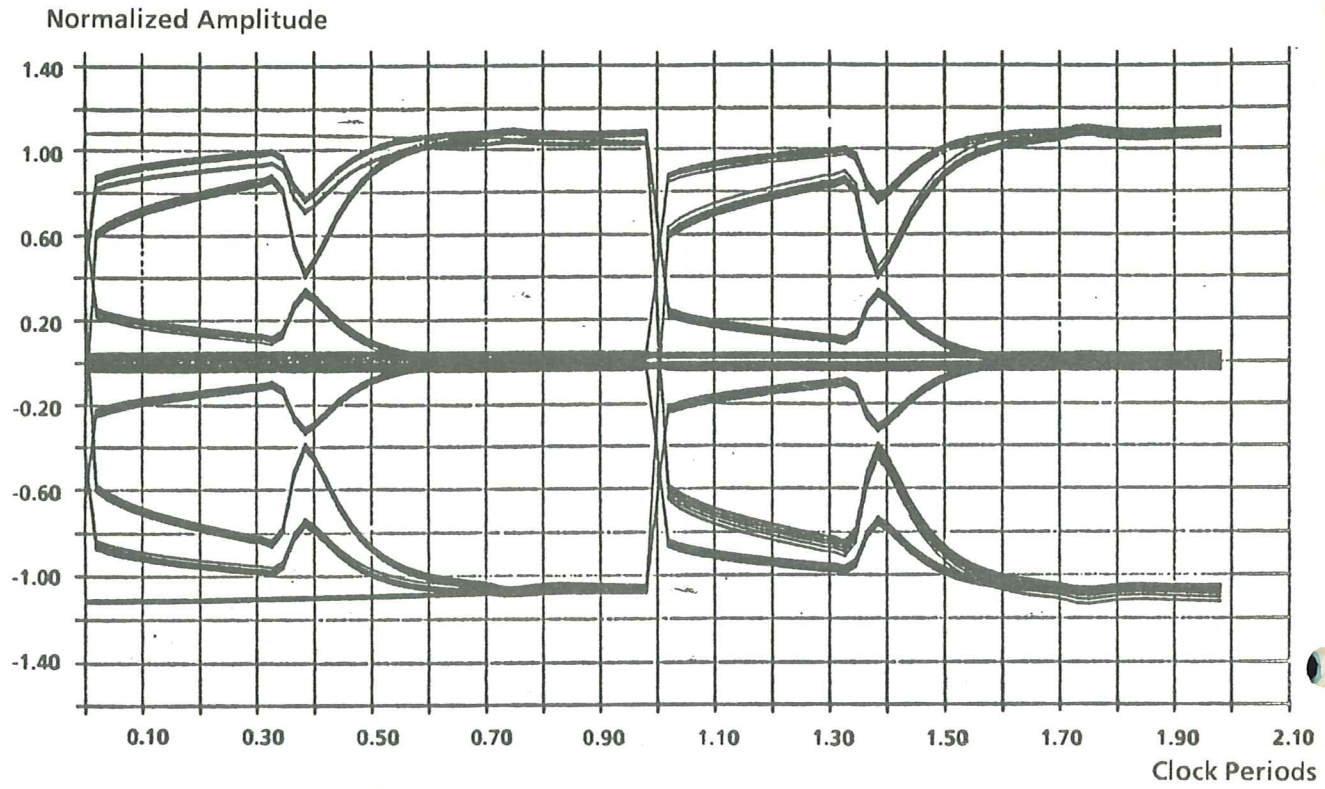


Figure 23 - Waveform of Test Configuration IIIa :
Short Passive Bus with 1 TE near to the PT, and 7 TEs at the far End
(C = 120 nF/km)

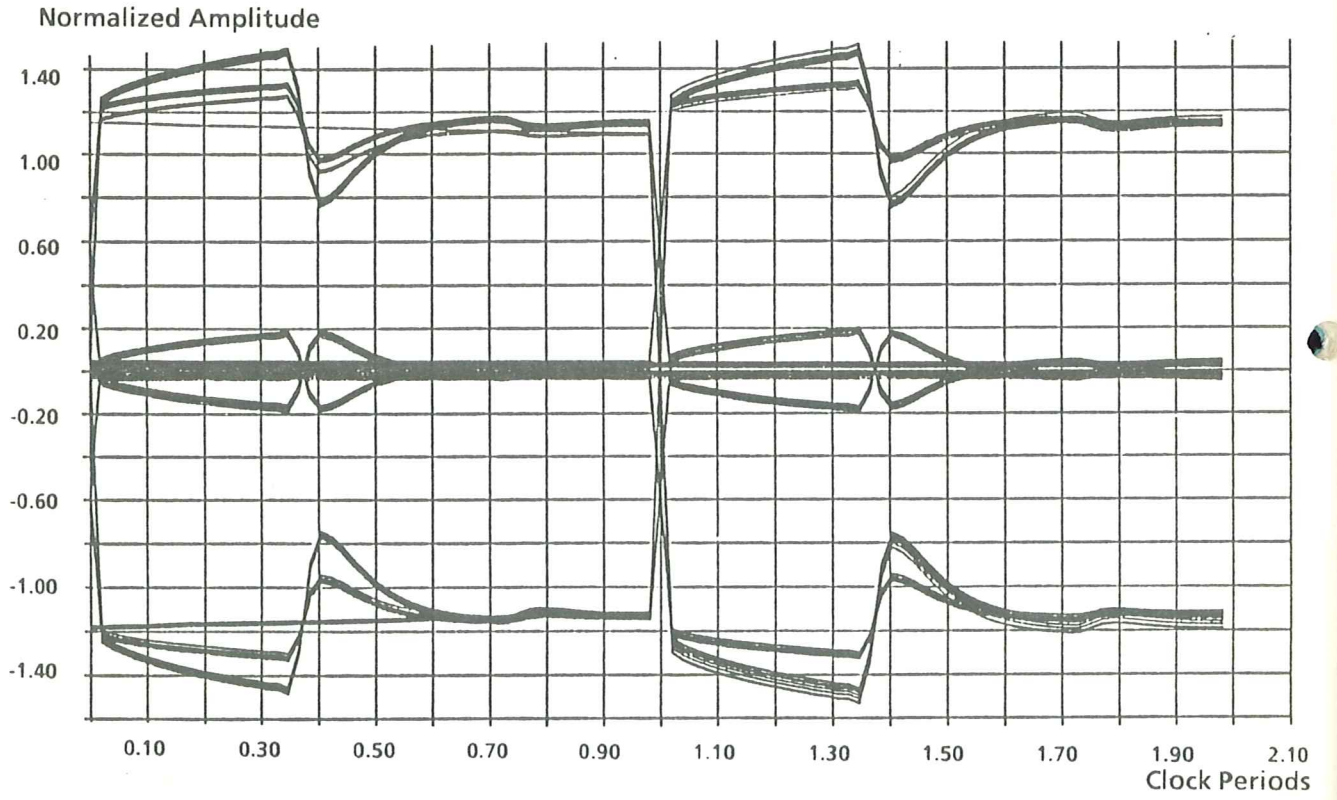
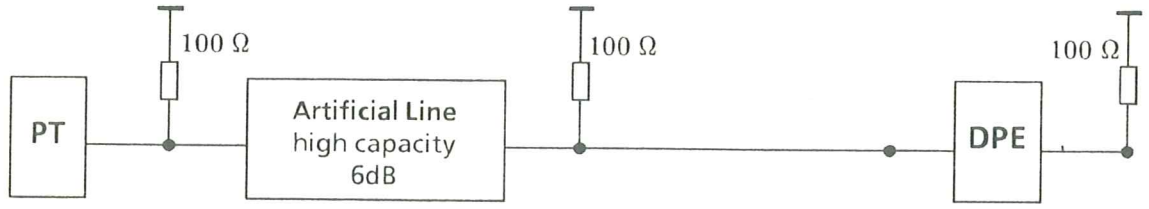
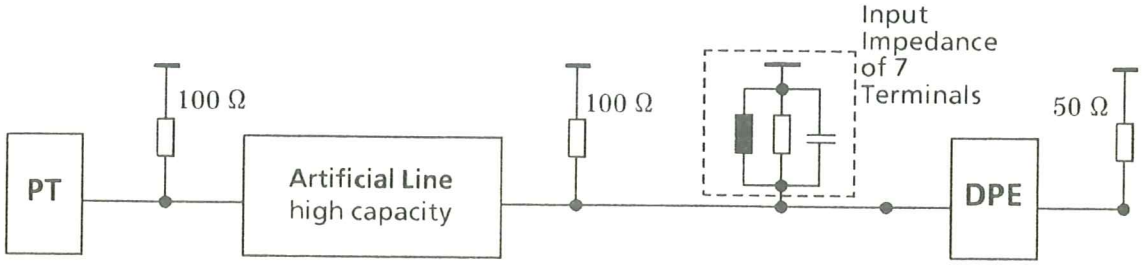


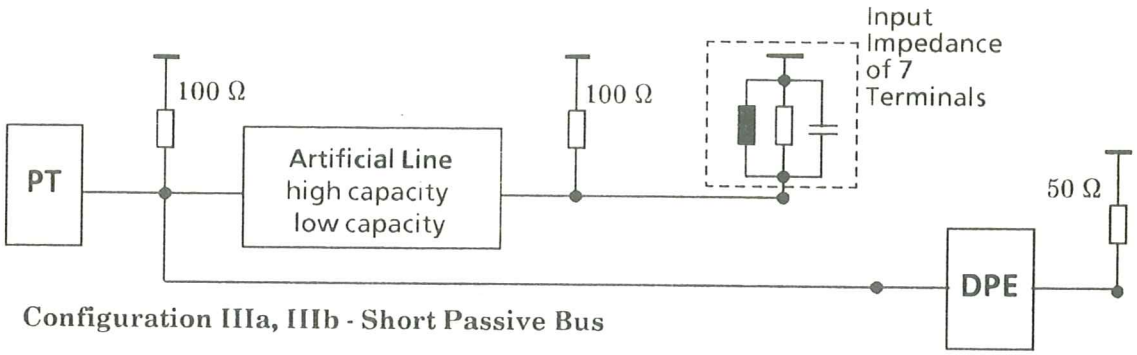
Figure 24 - Waveform of Test Configuration IIIb :
Short Passive Bus with 1 TE near to the PT, and 7 TEs at the far End
(C = 30 nF/km)



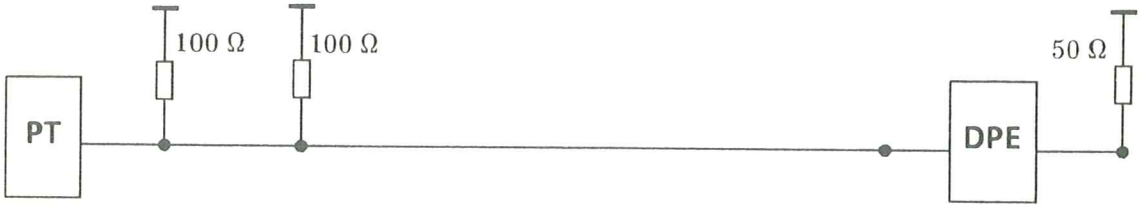
Configuration I - Point-to-Point



Configuration II - Short Passive Bus



Configuration IIIa, IIIb - Short Passive Bus



Configuration IV - Ideal Test Signal

Note:
The artificial lines are used to derive the waveforms. For test configurations II and III, the cable length corresponds to a signal delay of 1 µs. The parameters for the artificial lines are:

		High capacity cable	*Low capacitiy cable*
R	*(96 kHz)*	*160 Ω/km*	*160 Ω/km*
C	*(1 kHz)*	*120 nF/km*	*30 nF/km*
Z0	*(96 kHz)*	*75 Ω*	*150 Ω*
Wire diameter		*0.6 mm*	*0.6 mm*

Figure 25 - Test Configurations for the Generation of Waveforms

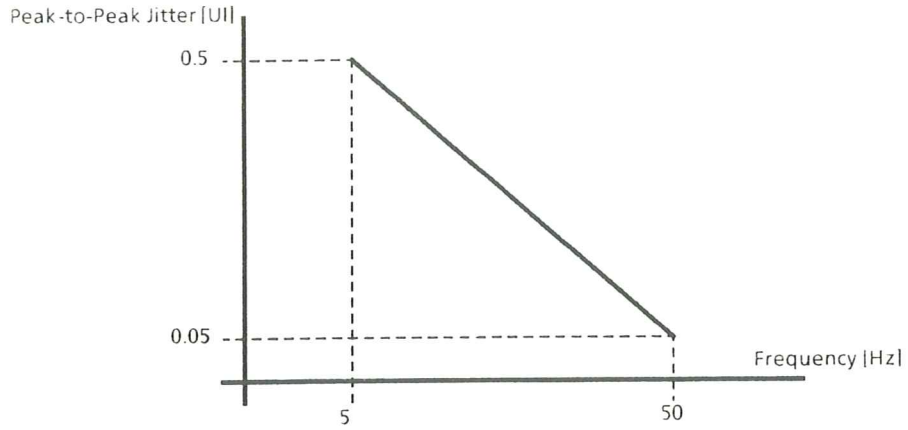
10.2.2 Timing Extraction Jitter

Timing extraction jitter due to the DPE shall be less than ±7% of a bit period when the jitter is measured using a high pass filter with a cut-off frequency of 30 Hz under test conditions described in 10.2.1. The bit patterns shall comply with CCITT Recommendations V.52 and V.57.

10.2.3 Total Phase Deviation

The total phase deviation (including effects of timing extraction jitter in the DPE) between the transitions of signal elements at the output of the DPE relative to the transitions of signal elements associated with the signal applied to the DPE input shall, for all bit positions, not exceed the range −7% to +15% of a bit period. For measurement purposes, the reference time scale used to define the signal element timing at the DPE input shall be derived from a reference point in each frame which is taken to be the crossing of Zero Volts which occurs between the framing pulse and its associated balance pulse.

The phase deviation shall be measured under all the test conditions described in 10.2.1 with the test patterns according to CCITT Recommendations V.52 and V.57 applied to the DPE input. Additionally, the limits shall be met when the test signal at the ouput of the pattern generator is modulated with sinusoidal jitter as given in Figure 26.



Legend: UI = Unit Interval

Figure 26 - Lower Limit of Maximum Tolerable Jitter at DPE Input (log/log-scale)

10.3 PT Jitter Characteristics

The maximum output jitter (p-p) shall be in accordance with CCITT Recommendation I.430.

10.4 Termination of the Line

The line impedance of the in-house cabling shall be in accordance with CCITT Recommendation I.430 [approximately 100 Ω; it will be terminated by a terminating resistor forming part of the in-house cabling (see Figure 27)].

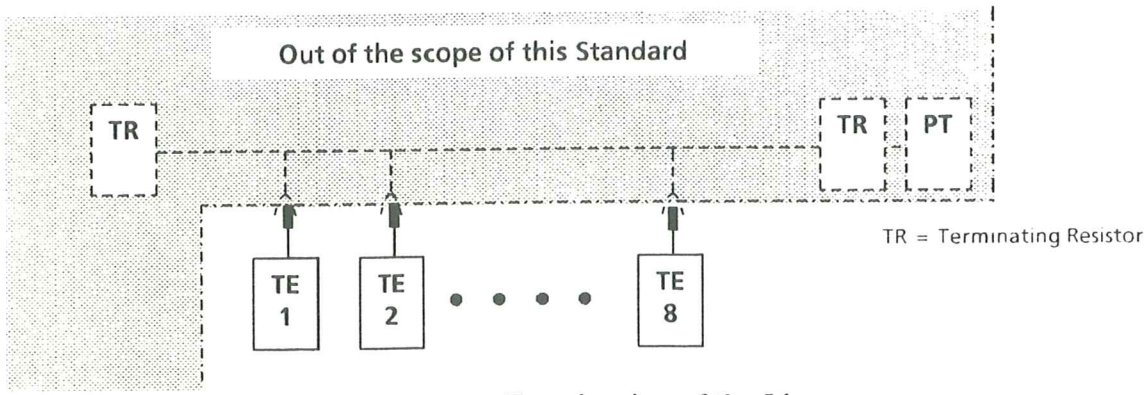


Figure 27 - Termination of the Line

10.5 DPE Output Characteristics

10.5.1 DPE Output Impedance

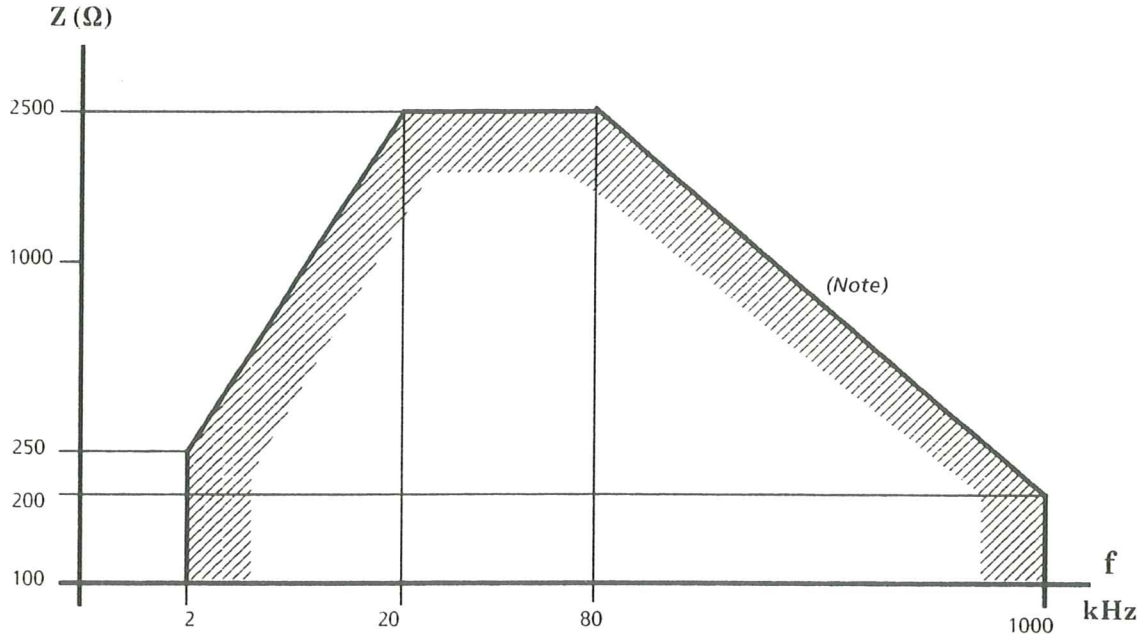
The following requirements for DPEs apply at the S_0 interface connector (see Figure 27):

A) When sending binary ONEs, the following requirements apply:

I The impedance, in the frequency range of 2 kHz to 1 MHz, should exceed the template in Figure 28. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV_{rms}.

II At a frequency of 96 kHz the peak current resulting from an applied voltage of up to 1.2 V_{peak} should not exceed 0.5 mA.

B) When sending binary ZEROs, the output voltage of the DPE will increase due to other TEs sending at the same time, eg. framing and D-channel bits. Attention is drawn to the requirement that the template shown in Figure 30 shall be met.



Note:
The slope corresponds to a capacitance load of 800 pF for the DPE including its connection cord and connectors.

Figure 28 - DPE Impedance Template, including Connection Cord and Plug

10.5.2 Test Load Impedance

Unless otherwise indicated, the test load impedance shall be 50 Ω.

10.5.3 Pulse Shape and Amplitude (binary ZERO)

10.5.3.1 Pulse shape

The pulse shape shall be within the mask of Figure 29.

10.5.3.2 Nominal Pulse Amplitude

The nominal pulse amplitude of a binary ZERO shall be ±750 mV.

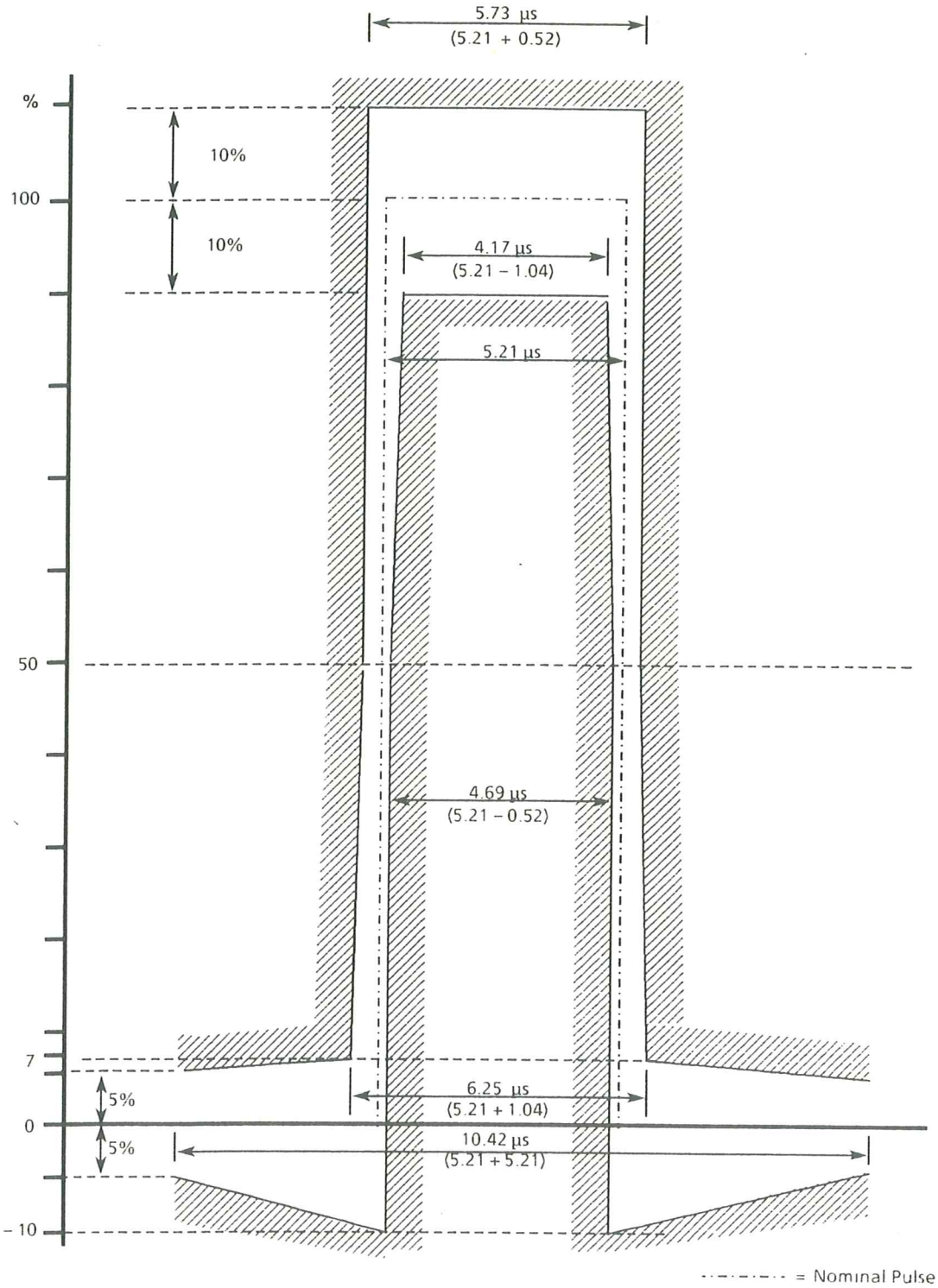
10.5.4 Pulse Unbalance

The pulse unbalance, ie. the difference between $\int V(t)dt$ for positive pulses and $\int V(t)dt$ for negative pulses, shall be ≤5%.

10.5.5 Voltage on Other Test Loads

10.5.5.1 The overvoltage with a load of 400 Ω shall be within the mask of Figure 30.

10.5.5.2 The voltage with a load of 5.6 Ω shall be ≤20% of the nominal pulse valtage.

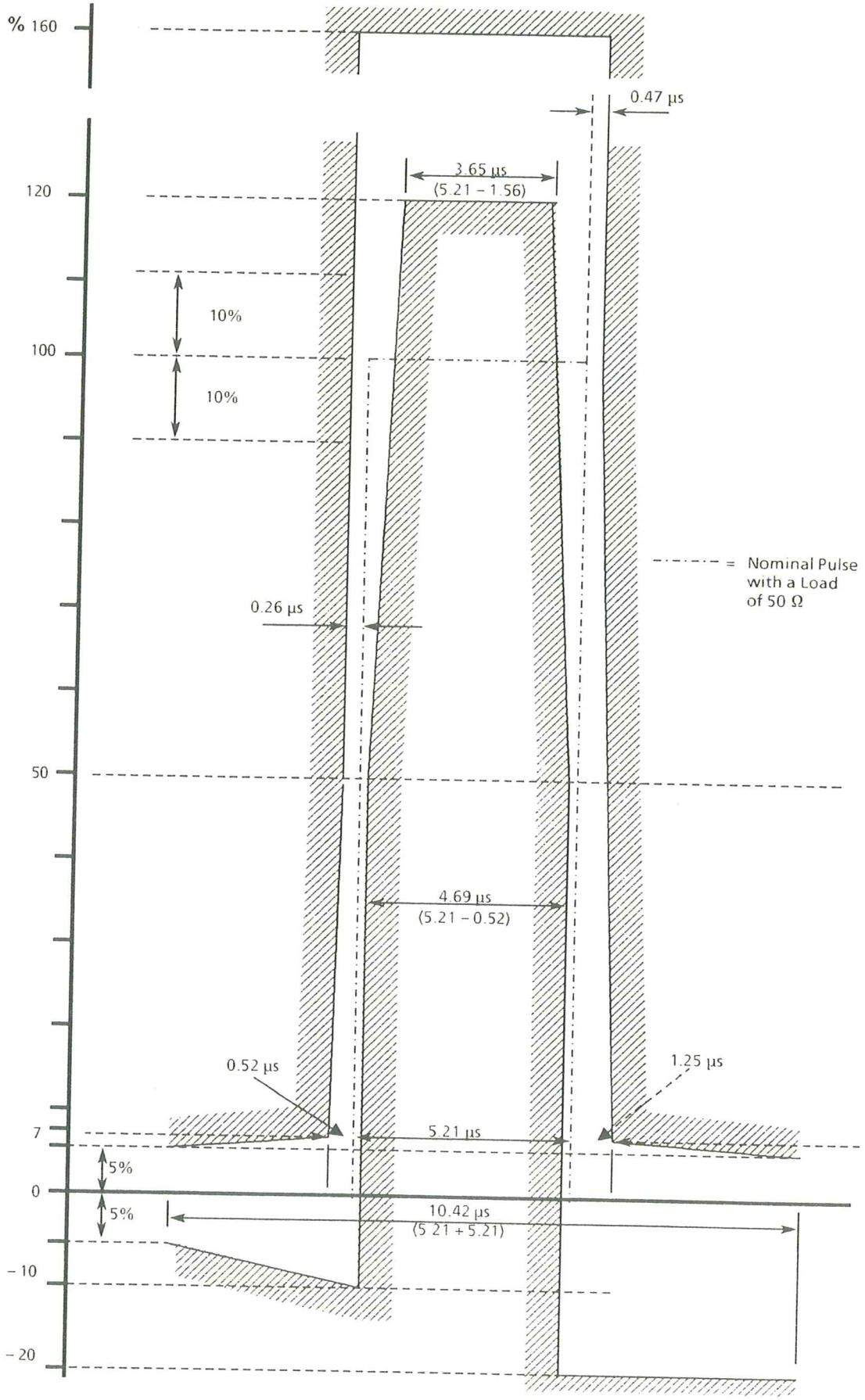


Note:
For the clarity of presentation the above values are based on a pulse length of 5.21 µs. The precise value can be derived from the bit rate given in 10.1.

Figure 29 - DPE Output Pulse Mask

10.5.6 Unbalance About Earth

The unbalance about earth is measured by considering the power feeding and two 100-Ω terminations at each port.

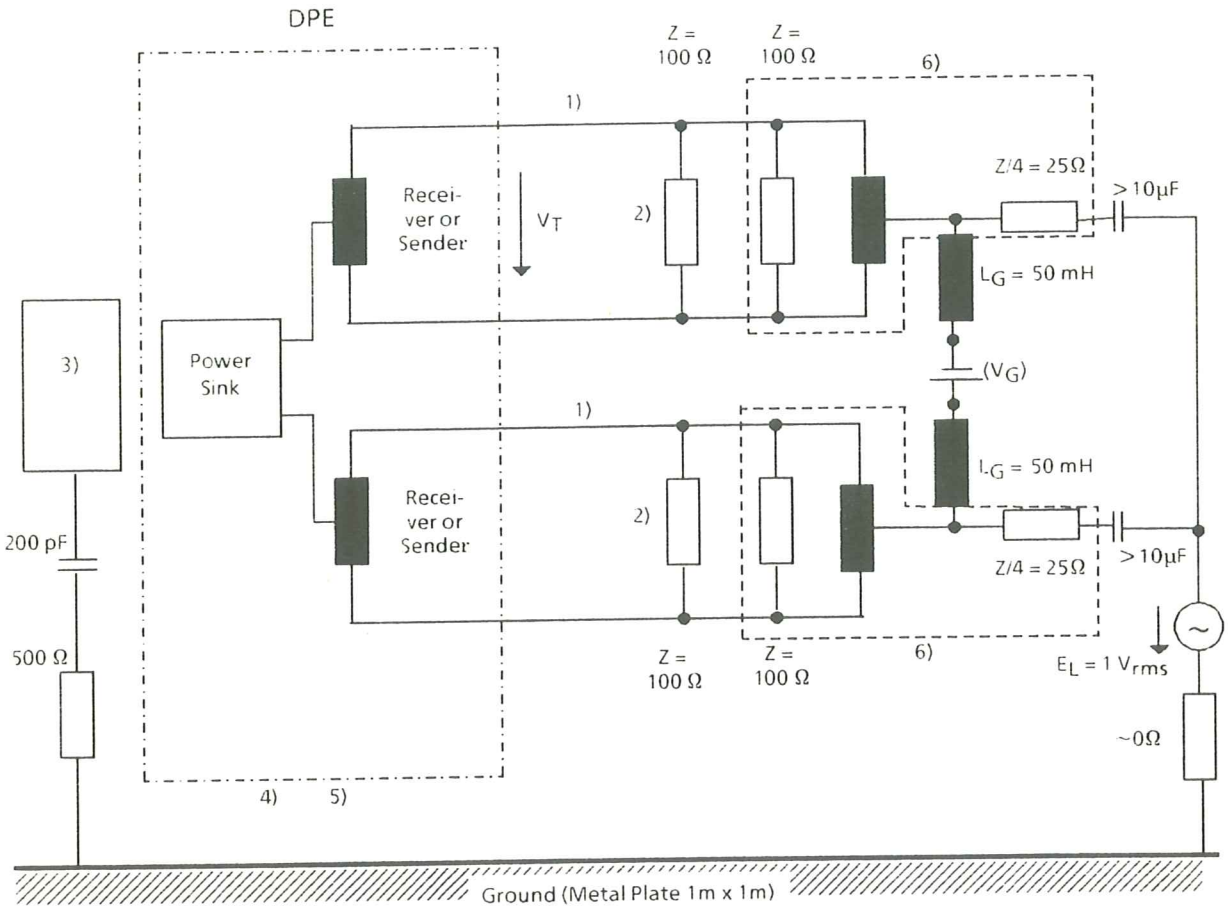


Note:
For the clarity of presentation the above values are based on a pulse length of 5.21 µs. The precise value can be derived from the bit rate given in 10.1.

Figure 30 - DPE Output Pulse Mask on a Test Load of 400 Ω

10.5.6.1 Longitudinal Conversion Loss (LCL)

The LCL shall be measured (see CCITT Recommendation G.117) in accordance with Figure 31 by considering power feeding and two 100-Ω terminations at each port.



Note 1: *The interconnecting cord shall lie on the metal plate.*
Note 2: *This resistor forms the terminating resistor.*
Note 3: *Hand imitation; a thin metallic foil with approximately the size of a hand.*
Note 4: *DPEs with a metallic housing shall have a galvanic connection to the metal plate. DPEs with non-metallic housings shall be placed on the metal plate.*
Note 5: *The power cord for mains powered DPEs shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.*
Note 6: *This circuit provides a transversal termination of 100 Ω and a balanced longitudinal termination of 25 Ω. Any equivalent circuit as given in CCITT Recommendations G.117 and O.121 is also acceptable.*

Figure 31 - Receiver Input or Sender Output Longitudinal Conversion Loss

The longitudinal conversion loss LCL, expressed in dB, is defined as:

$$LCL = 20 \cdot log \left| \frac{E_L}{V_T} \right|$$

The voltages V_T and E_L shall be measured within the frequency range from 10 kHz up to 1 MHz by employing a selective test equipment.

The measurements shall be carried out in the states:

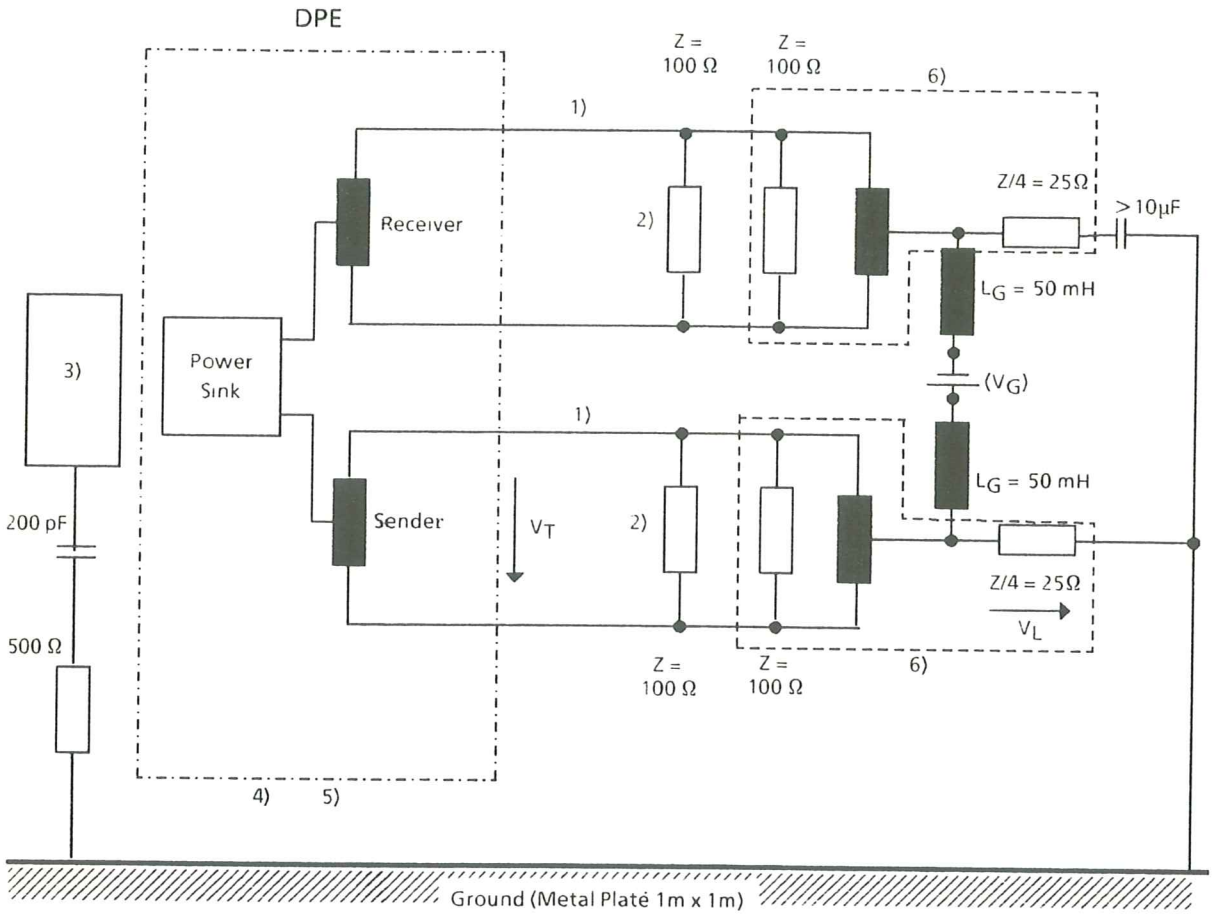
F3 DEACTIVATED (receiver and sender)
F1 POWER-OFF (receiver and sender).

The longitudinal conversion loss shall be in the range

a)	10 kHz < f < 300 kHz	≥54 dB
b)	300 kHz < f < 1 MHz	≥54 dB, decreasing with 20 dB/decade.

10.5.6.2 Output Signal Balance (OSB)

The OSB shall be measured (see CCITT Recommendation G.117) in accordance with Figure 32 by considering the power feeding and two 100-Ω terminations at each port.



Note 1: *The interconnecting cord shall lie on the metal plate.*
Note 2: *This resistor forms the terminating resistor.*
Note 3: *Hand imitation; a thin metallic foil with approximately the size of a hand.*
Note 4: *DPEs with a metallic housing shall have a galvanic connection to the metal plate. DPEs with non-metallic housings shall be placed on the metal plate.*
Note 5: *The power cord for mains powered DPEs shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.*
Note 6: *This circuit provides a transversal termination of 100 Ω and a balanced longitudinal termination of 25 Ω. Any equivalent circuit as given in CCITT Recommendations G.117 and O.121 is also acceptable.*

Figure 32 - Sender Output Unbalance about Earth

The output signal balance, expressed in dB, is defined as:

$$OSB = 20 \cdot log \left| \frac{V_T}{V_L} \right|$$

The voltages V_T and V_L shall be measured within the frequency range from 10 kHz up to 1 MHz by employing selective test equipment. The measuring shall be carried out in a maintenance state under the normal power consumption condition, see 11.2. The pulse patterns shall be all binary ZERO, see 9.3.1.

The output signal balance shall be:

a)	at 96 kHz	≥54 dB
b)	96 kHz < f < 1 MHz	≥54 dB, decreasing with ≤20 dB/decade

10.6 DPE Input Characteristics

10.6.1 DPE Receiver Input Impedance

DPEs shall meet the requirements specified in 10.5.1 (A).

10.6.2 Receiver Sensitivity, Noise and Distortion Immunity

DPEs shall receive without errors (for a period of at least one minute) an input with a pseudo random sequence (word length ≥511 bits) in all information channels (combination of B-channel and D-channel).

The receiver shall operate with any input sequence over the full range indicated by the wave form mask as generated according to 10.2.1. In addition, for a wave form generated according to test configuration "I" (see Figure 24) a sinusoidal signal with an amplitude of 150 mV_{p-p} at frequencies of 200 kHz and 2 MHz shall be individually superimposed on the input signal.

10.6.3 Unbalance About Earth

The Longitudinal Conversion Loss shall be measured by considering the power feeding and two 100-Ω terminations at each port as indicated in Figure 30 (see also CCITT Recommendation G.117).

a)	10 kHz < f < 300 kHz	≥54 dB
b)	300 kHz < f < 1MHz	≥54 dB, decreasing with ≤20 dB/decade

10.7 Isolation from External Voltages

See Standard ECMA-57.

11 Power Feeding

11.1 Reference Configuration

Although an 8-pole connector is to form a universal CCITT S_0 interface (see CCITT Recommendation I.430), the ECMA reference configuration uses the four access leads 3, 4, 5 and 6 only, as depicted in Figure 33. The use of the leads 1, 2, 7, and 8 is outside the Scope of this Standard.

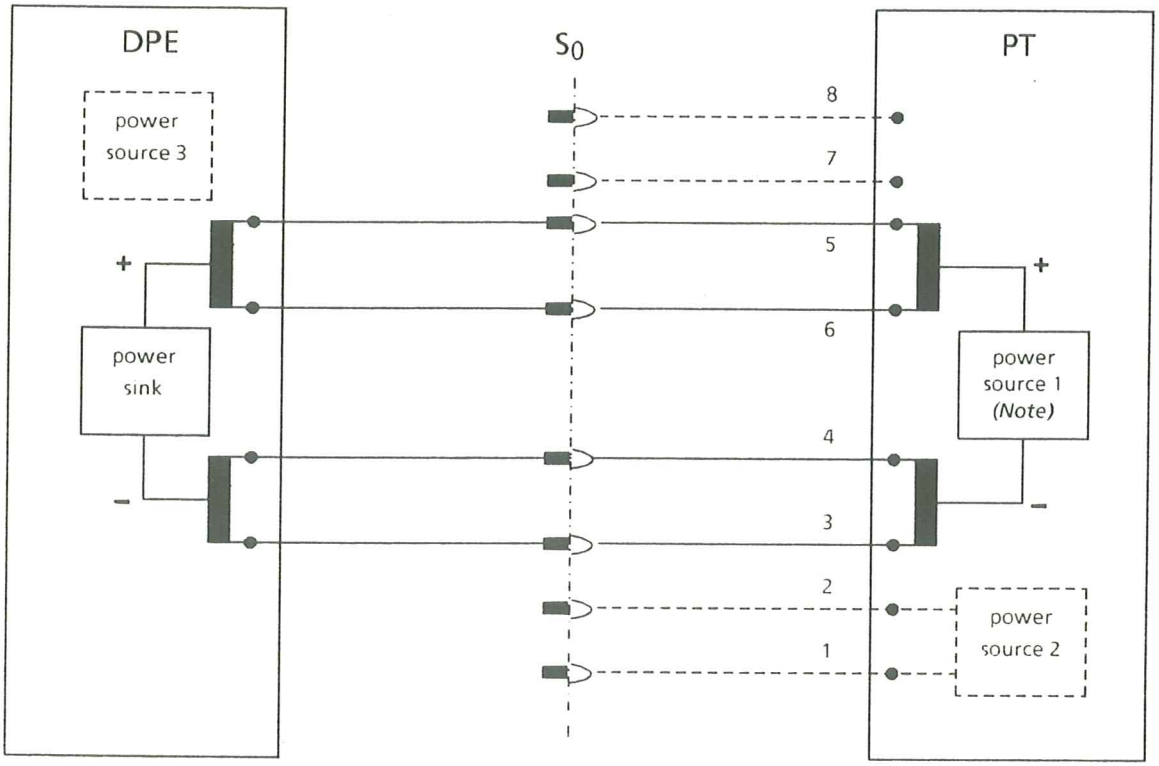
Note:
The numbering of the leads does not imply any assumption on pin allocation of physical connectors.

11.1.1 Functions Specified for the Access Leads

The access leads 3-4 and 5-6, used for the bi-directional transmission of the digital signal, provide a phantom circuit for power transfer from the PCSN to the DPE (power source 1 / power sink).

11.1.2 Provision of Power Sources

The DPE (power sink) may be powered by power source 1 or by power source 3.



Note:
The polarity of the voltage of power source 1 refers to the normal powering condition. Under emergency conditions the polarity is reversed.

Figure 33 - Power feeding via the S_0 interface

Power source 1 may not always be provided.

Note: A terminal that is to be portable (for example from PCSN to PCSN, country to country) cannot rely exclusively on phantom power for its operation.

Power source 2 is outside the Scope of this Standard.

Power source 3 may be by batteries and/or by mains.

11.2 Power Available at the DPE from Power Source 1

With power source 1, two situations are considered, "normal" and "emergency".

When the PT enters a state where it is only able to supply emergency power, this will be indicated by reversing the polarity of power source 1. In this condition only a reduced set of terminal functions is allowed to consume power from power source 1.

Under normal conditions, the power available depends on the implementation of the PCSN. It should, however, exceed the power available under the emergency condition.

Under emergency conditions, the minimum power available from power source 1 to be shared among all TEs will be 400 mW.

The voltage will be 40 V_{DC} +5% / –20%, when drawing the maximum available power.

11.3 Power Consumption in the DEACTIVATED State

In this case, the power consumption of all TEs on a bus shall not exceed 100 mW.

Note:
After an interim period, this value is likely to be reduced to 25 mW under emergency conditions.

11.4 Current Transients

The rate of change of current drawn by a DPE (eg. when being connected or as a result of a polarity change for indication of the emergency condition) shall not exceed 5 mA/µs.

12 Physical Characteristics

12.1 Connectors

The connectors (including their pin allocation) shall be as defined for use at the ISDN basic user-to-network interface (at the S reference point).

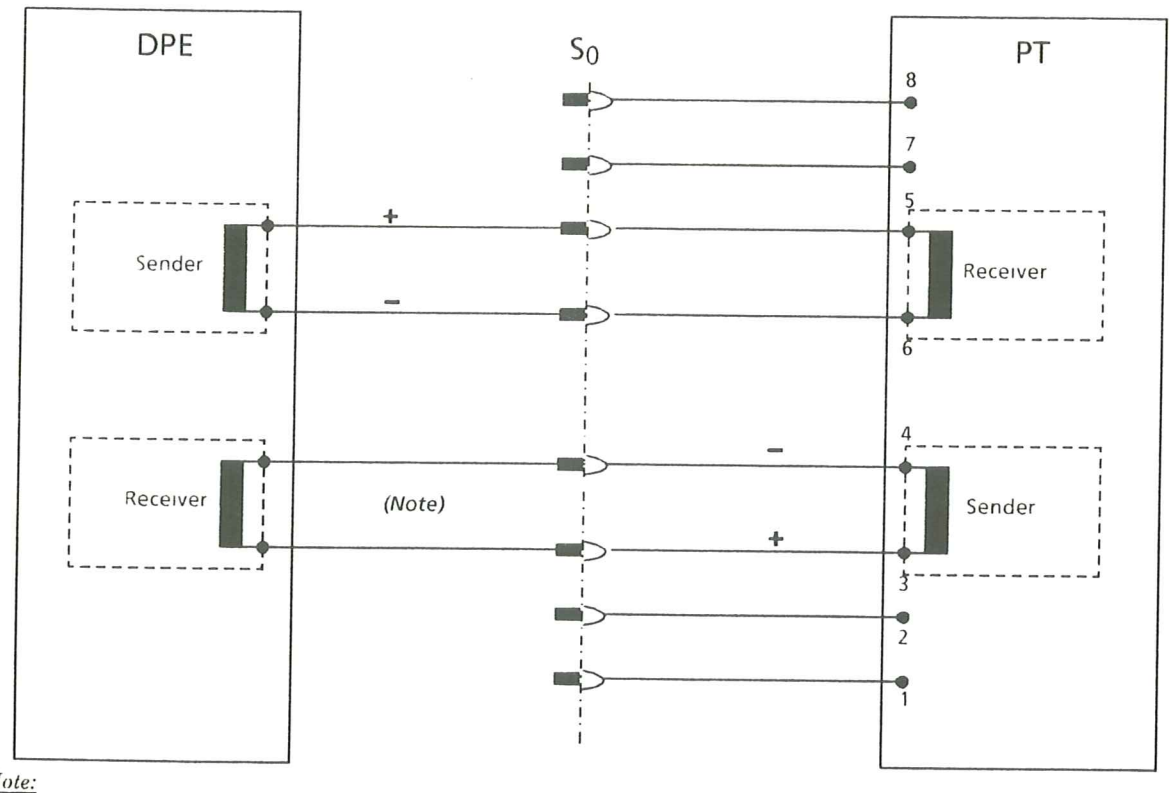
12.2. Connection Cord

For the electrical characteristics of the connection cord see Chapter 10. Other characteristics are specified below.

12.2.1 Use of the Access Leads

As shown in Figure 34, the PCSN will provide a one-to-one mapping between the outlets of the S_0 female connector(s) and its PT (however, see 6.3 for possible polarity reversal). The connection cord shall provide four access leads fitting to the leads 3 to 6 of the PCSN wiring.

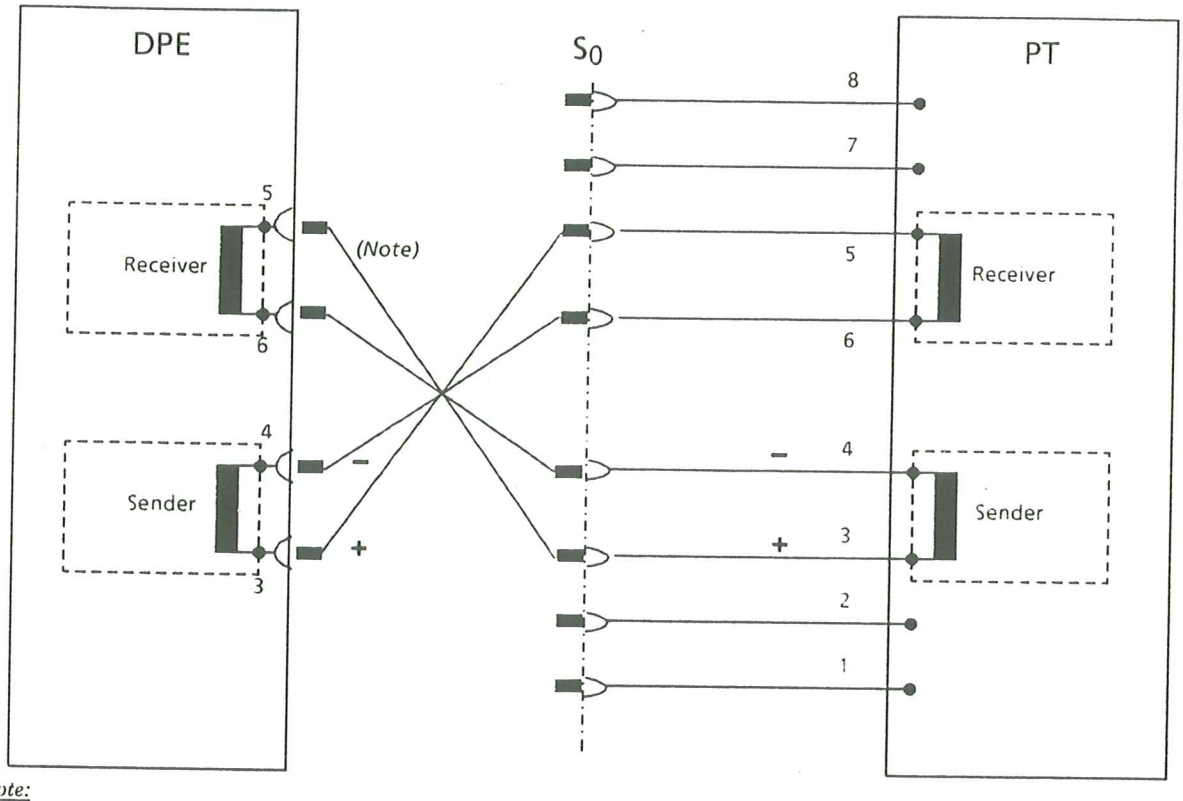
When the connection cord is fixed to the DPE, its access leads used for the transmission of signals to the PCSN shall connect to the PCSN wires 5 and 6 while its access leads used for the reception of signals from the PCSN shall connect to the PCSN wires 4 and 3, see Figure 35.



Note:
Due to possible reversion of the two wire interchange circuit (see 6.3), the bits may be received with opposite polarity.

Figure 34 - Use of the S_0 Interface Access Leads, with the Connection Cord fixed to the DPE.

When the connection cord is pluggable at the DPE, it shall interchange its wires as shown in Figure 35.



Note:
Due to possible reversion of the two wire interchange circuit (see 6.3), the bits may be received with opposite polarity.

Figure 35 - Use of the S_0 Interface Access Leads, the Connection Cord being pluggable at the DPE.

12.2.2 Signal Polarity of the Access Leads

A positive pulse (eg. a framing pulse) transmitted by the DPE is defined with a positive voltage of the PCSN access lead 5 relative to PCSN access lead 6, see Figure 34.

If the wiring polarity is maintained, a positive pulse (eg. a framing pulse) received by the DPE will occur as a positive voltage between PCSN access leads 3 and 4, see Figure 34.

12.2.3 Length of the Connection Cord

The length of the connection cord shall not exceed 10 m.

APPENDIX

Acronyms

AMI	Alternate Mark Inversion
DPE	Data Processing Equipment
IWU	Interworking Unit
LCL	Longitudinal Conversion Loss
MPH-EI	Management/Physical Layer Error Indication
MPH-ES	Management/Physical Layer Error Response
MPH-LAI	Management/Physical Layer Loop Activation Indication
MPH-LDI	Management/Physical Layer Loop Deactivation Indication
MPH-LAR	Management/Physical Layer Loop Activation Request
MPH-LDR	Management/Physical Layer Loop Deactivation Request
MPH-AI	Management/Physical Layer-Activate Indication
MPH-AR	Management/Physical Layer-Activate Request
MPH-DI	Management/Physical Layer-Deactivate Indication
MPH-DR	Management/Physical Layer-Deactivate Request
MULDEX	Multiplexer/Demultiplexer
OSB	Output Signal Balance
PCSN	Private Circuit Switching Network
PH-AI	Physical Layer-Activate Indication
PH-AR	Physical Layer-Activate Request
PH-DI	Physical Layer-Deactivate Indication
PT	PCSN Termination at the S reference point
SDL	Specification and Description Language
TE	Terminal Equipment